96768300

CONTROL DATA CORPORATION

CDC® CYBER 18 PROCESSOR WITH MOS MEMORY

MACRO LEVEL

SYSTEM DESCRIPTION
FUNCTIONAL DESCRIPTION
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INTERRUPT SYSTEM
PROGRAM PROTECT
I/O DEVICES

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LIST OF EFFECTIVE PAGES

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PREFACE

The micro-programmable processor emulates the 1700 family of computers. Readers of this document should be familiar with the CDC® 1700 Series computers and their associated hardware. The processor is upward-compatible and has an enhanced instruction capability.

Additional information on CDC software applicable to the micro-programmable processor system can be found in the following publications:

Description	Publication Number
1700 Computer System Codes	60163500
Mass Storage Operating System (MSOS) Version 5 Reference Manual	96769400
MS FORTRAN Version 3A/B Reference Manual	60362000
CYBER 18 Processor with Core Memory (Macro Level) Reference Manual	88973400
CYBER Cross System Version 1 (under SCOPE) Micro Assembler Reference Manual	88988800
CYBER Cross System Version 1 (under SCOPE) Macro Assembler Reference Manual	88988900
CYBER Cross System Version 1 (under NOS and NOS/BE) Micro Assembler Reference Manual	96836400
CYBER Cross System Version 1 (under NOS and NOS/BE) Macro Assembler Reference Manual	96836500
TIMESHARE Version 3 Reference Manual	96768000
Operational Diagnostic System (ODS) Reference Manual	39452100

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TABLES

The 1700 enhanced processor is a special configuration of the CDC micro-programmable processor family of parallel mode, stored program, digital processors. It is dedicated to perform as a 1700-compatible digital computer. The processor uses micro programming to execute the basic 1700 instruction repertoire plus additional enhanced instructions.

This manual describes the basic, as well as the optional, characteristics of the processor. It covers the hardware, general operating procedures, and processor instruction repertoire.

The basic processor configuration consists of:

- Micro processor with 1700 transform
- Micro memory (read-only memory)
- Main memory (MOS)
- Input/output interface
- Power supply

Various standard options, such as a card reader and a line printer, are available for the CYBER 18 Computer System. The user may also use the micro memory and input/output to perform nonstandard 1700 functions to achieve even greater flexibility with the processor.

The MOS main memory differs from core main memory in operation. Although all core memory instructions can be used with MOS memory, additional instructions are available for MOS memory only. Page mode memory instructions permit up to 512K bytes to be accessed. Page mode addressing is discussed in section 2 under Main Memory Configuration. Page register loading and statusing instructions begin in the section entitled Miscellaneous Instructions in section 4.

In addition, the MOS main memory is optionally available with error checking and correction (ECC). ECC automatically corrects single-bit memory errors and provides parity error indication only on double-bit errors. The ECC status instruction is explained under Miscellaneous Instructions in section 4. However, it is normally needed only in diagnostic routines. In ordinary memory references, ECC operation in the memory is transparent to the processor.

A listing of the general processor characteristics is contained in table 1-1.

FUNCTIONAL CHARACTERISTICS

The micro-programmable computer is a multilevel processor that uses a semiconductor read-only memory and a special hardware function (transform) to emulate a CDC 1700 computer. The main memory unit contains 1700 language programs (called macro instructions). The multilevel processor differs from the conventional processor, as shown in figure 1-1. Processor operation is controlled by a micro program in micro memory. The micro program reads 1700 macro instructions from main memory and decodes them for execution in the micro processor. The micro memory is several times faster than the main memory. The transform aids in decoding and program execution. Therefore, the processor uses special micro-programming techniques to emulate an enhanced 1700 system for lower cost, smaller size, and overall better performance.

PHYSICAL CHARACTERISTICS

The processor is modularly designed with standard TTL MSI components and commercial construction.

The standard chassis, shown in figure 1-2, is 18.5 in. (46.99 cm) high by 17.5 in. (44.79 cm) wide by 12 in. (30.48 cm) deep. The chassis includes cooling fans and a front cover panel. The standard chassis back panel has the input/output wiring for the 1700 A/Q and 1700 A/Q-DMA. However, it may also contain specialized input/output for the user. Wiring details are included in the system wirelist provided with the unit.

Power requirements for the processor vary with the user's application. Power supplies of ±5 and ±12 volts are included in a separate chassis. Physical dimensions for the power supply chassis are 8.75 in. (22.22 cm) high by 17.5 in. (44.79 cm) wide by 16.0 in. (40.64 cm) deep. Processor input power is 120 V ac, 50 or 60 Hz.

A typical processor printed wiring assembly, shown in figure 1-3, is 11 by 14 in. (27.94 by 35.56 cm) and has 204 input/output contracts.

The processor chassis has a prewired location for an optional breakpoint panel interface card. The breakpoint panel is a 16-in. (40.64-cm) by 4.5-in. (11.43-cm) printed circuit board, connected by a flexible cable to the panel interface printed wiring assembly. The panel contains controls and light emitting diode indicators for manually controlling the processor at the micro level. The breakpoint controller printed wiring assembly also provides an interface to ASCII RS232-compatible consoles (full-duplex interface) for control of the processor. The console display normally attaches to the RS232 serial interface on the I/O-TTY module. A teletypewriter-compatible current loop interface is also available.

The processor operates in computer rooms, general offices, and industrial environments. It operates at temperatures of 40°F to 120°F (4.5°C to 48.8°C), withstands a maximum temperature gradient of 18°F (10°C) per hour or at a rate that precludes condensation, and a relative humidity of 10 to 90 percent. Nonoperating environment extends the temperature range from -30°F to 150°F (-35°C to 65°C) and a

TABLE 1-1. PROCESSOR GENERAL CHARACTERISTICS

Category	Description
Basic Configuration	
Processor	
Type	General-purpose, micro-programmable digital processor
Organization	Register oriented or file oriented
Word length	16 bit
Micro-instruction word	Two 32-bit micro instructions per micro-memory word
Micro-memory type	Semiconductor read-only memory standard; read/write memory optional
Micro-memory size	512 words of read-only memory on transform; up to 4096 additional words of random access memory optional
Micro-memory access time	70 nanoseconds
Arithmetic	Binary with dynamic selection of ones or twos complement mode
	Up to four parallel, unrelated operations are possible in one micro instruction
Micro-instruction execution time	An average of 1 microsecond cycle time (for detailed timing, see appendix C).
Main Memory	
Size	Variable, according to application: 32K bytes; 256K bytes (one processor)/512K bytes (two processors)
Type	N-Channel Dynamic MOS (4K chips)
	Parity and protect bits included. Automatic single-bit error correction optional (to 196K bytes/processor)
Speed	Read: 600 nanoseconds cycle time† Write: 700 nanoseconds cycle time†
Direct memory access (DMA)	Four input/output ports are wired for DMA devices.
Input/Output	
Interfaces	Teletypewriter Console display (RS232-C compatible)
Mechanical	
Hardware	Modular
Construction	RETMA 19-inch, rack mountable

†The shortest possible time between successive operations

TABLE 1-1. PROCESSOR GENERAL CHARACTERISTICS (Contd)

Category	Description
Dimensions	Logic Chassis: Height – 18.5 in. (47 cm) Width – 17.5 in. (44.5 cm) Depth – 16.0 in. (40.64 cm) Power Supply Chassis: Height – 8.75 in. (22.25 cm) Width – 17.5 in. (44.5 cm) Depth – 16.0 in. (40.64 cm)
Weight	Logic Chassis: 40 lbs (approximately) 18 kg) Power Supply: 50 lbs (approximately) 45 kg)
Input power	120 bolts, 50/60 Hz, 15 amperes
Miscellaneous features	Real-time clock Auto-data transfer Enhanced 1700 instruction repertoire
Standard Options	
Input/Output	
Interfaces	Breakpoint panel RS232-C compatible console
Operator input device	Teletypewriter ASR/KSR 33/35 CDC console displays (RS232-C compatible)

maximum thermal gradient not to exceed 20°F per hour or at a rate that percludes condensation. Storage temperatures with proper packaging protection may range from -60°F to 160°F (51.1°C to 71.1°C) and relative humidity from 2 to 98 percent with temperature cycles of not more than 60°F per hour or at a rate that precludes condensation. The user should note that these ranges cover only the micro processor; peripheral equipments may require more stringent environmental controls.

MAJOR SYSTEM COMPONENT DESCRIPTION

Figure 1-4 shows the chassis layout for the standard processor equipment; figure 1-5 is the functional block diagram.

MICRO PROCESSOR

The enhanced processor consists of an arithmetic logical unit (ALU) printed wiring assembly, a status mode interrupt (SMI) printed wiring assembly, control printed wiring assemblies 1 and 2, and a 1700 transform printed wiring assembly. The microprocessor cards are interconnected through the basic backpanel wiring. Special user options require additional wiring.

TRANSFORM

The transform hardware is packaged as a separate printed wiring assembly and is specially designed for processor application. The processor has a 512-word, 64-bit read-only micro memory on the transform module.

Functioning as the hardware portion of the macro-instruction decode process, the transform causes the micro program to form program branches, set various parameters, and perform arithmetic or logical operations. It provides the micro program with the capability of selecting patterns of bits from the data transmission paths to form the micro-memory addresses that sequence the micro program.

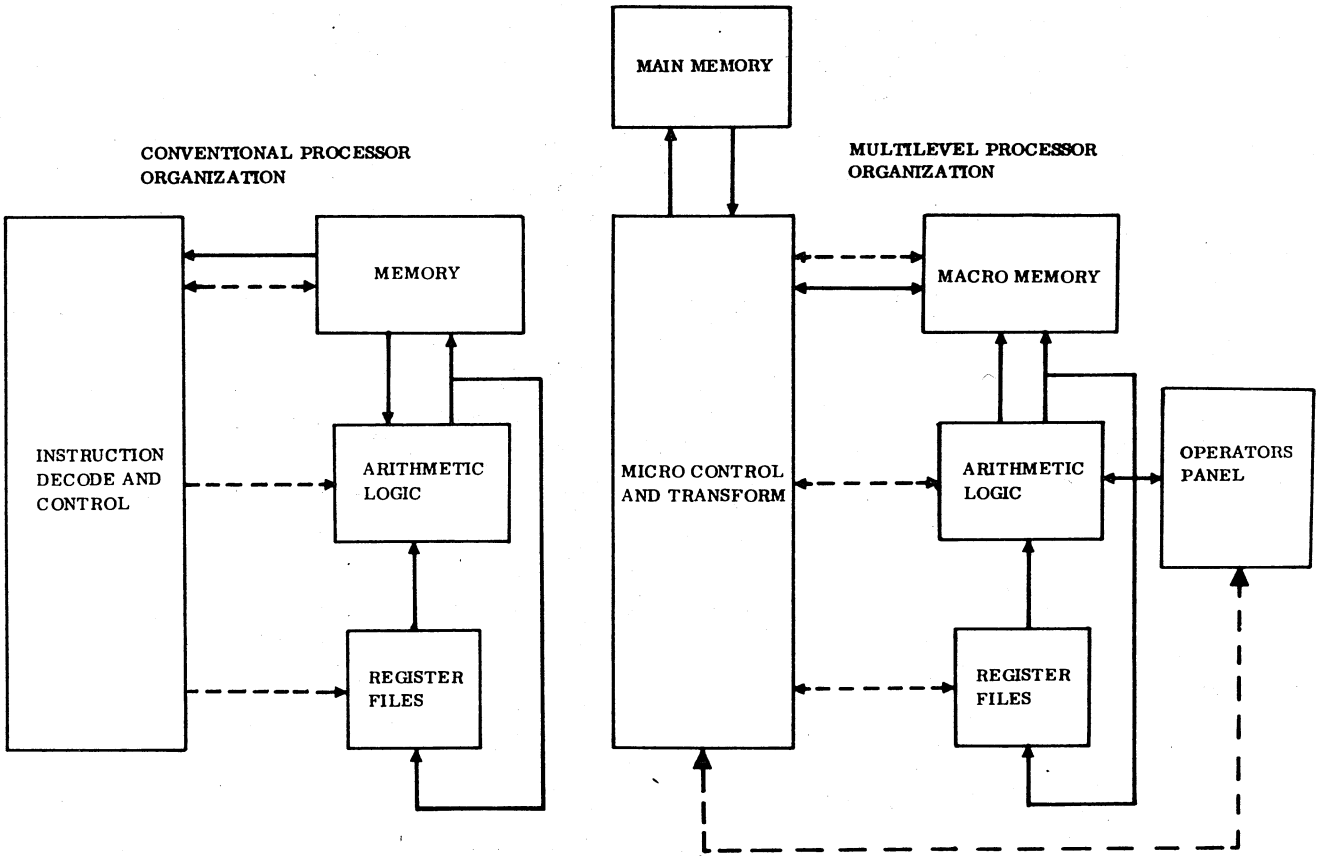


Figure 1-1. Digital Processor Organizations

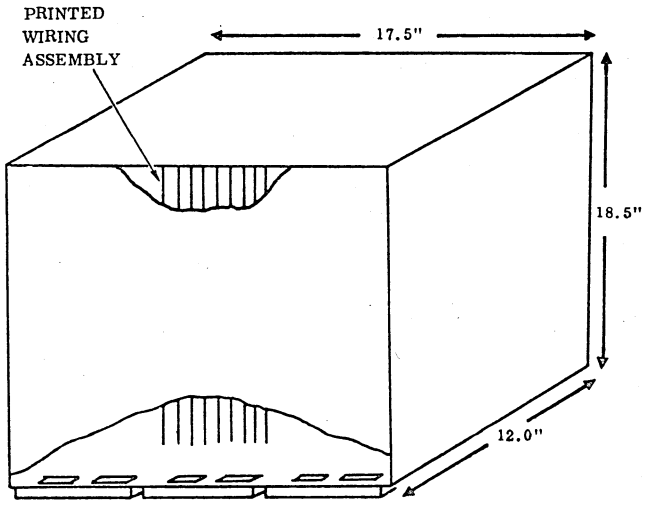


Figure 1-2. Standard Processor Chassis

MICRO MEMORY

The processor contains a 512-word micro memory on the 1700 transform board. It also has two printed wiring assembly slots for additional micro-memory or special algorithms if required by the user. The slots are interconnected to the micro processor through the backpanel and are accessible only by the micro processor.

MAIN MEMORY (MOS) AND MEMORY INTERFACE

The MOS main memory consists of MOS memory array modules and two interface modules. The memory array modules are configured in 16K or 32K increments of 18 bits: 1 parity, 1 protect, and 16 data bits. The interface and memory array modules are standard 11-in. by 14-in. (27.94-cm by 35.56-cm) circuit boards.

Data flow is in 16-bit word format, with a maximum of 131k words possible in the basic chassis. A direct memory access (DMA) channel is included in the memory interface as well

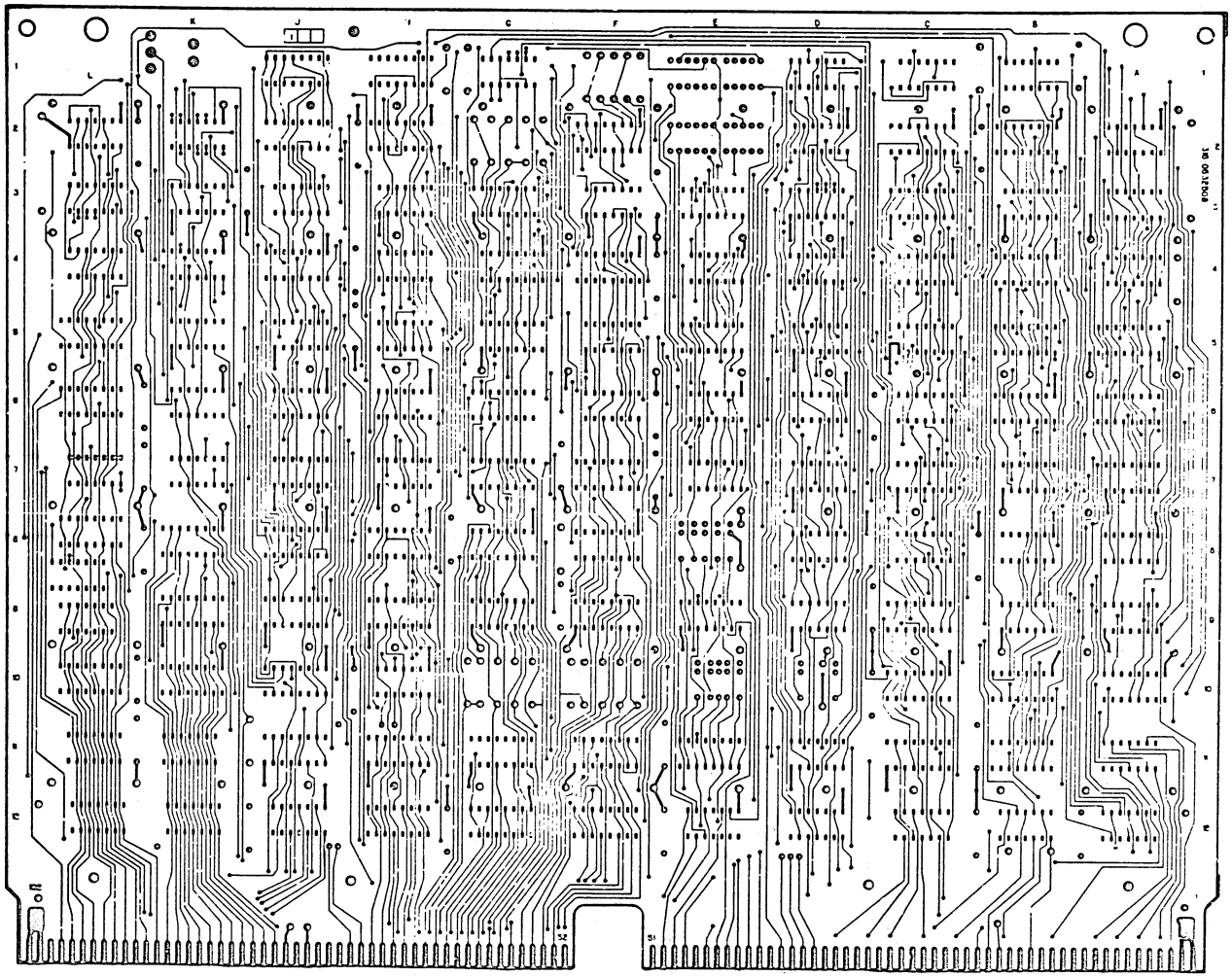


Figure 1-3. Typical Processor Printed Wiring Assembly

as the parity and program protect generation and checking. The DMA for the processor can provide access for four external DMA devices through a port to main memory.

I/O-TTY INTERFACE

The standard operator interface to the processor is through the I/O-TTY module. It can interface with a Teletype Corporation Model ASR/KSR 33/35 Teletype or the CONTROL DATA RS232-C compatible console display. A TTL bus is available in the I/O-TTY module for interfacing the controllers in the main chassis to the micro processor.

EXTERNAL I/O INTERFACE

The main chassis for the processor includes 11 slots for external input/output devices (in addition to the input/output capability of the I/O-TTY module). Printed wiring assembly slot assignments in the processor chassis are shown in figure 1-4. Four slots are prewired for 1700 A/Q-DMA channels, and five slots are prewired for 1700 A/Q channels:

1700 A/Q-DMA channels: Slots A, D, G, H

1700 A/Q channels: Slots AA, C, E, F, J

These may be used with standard CDC equipment or for special user applications.

AB113-A PROCESSOR (CYBER 18-20/30 TIMESHARE)

16/32K MOS MEMORY (OR ERROR CHECKING AND CORRECTION†)	AC
16/32K MOS MEMORY†	Z
16/32K MOS MEMORY†	Y
16/32K MOS MEMORY†	X
MOS MEMORY ADDRESS/CONTROL INTERFACE	W
MOS MEMORY DATA INTERFACE	V
PANEL INTERFACE†	U
MICRO MEMORY†	T
MICRO MEMORY†	S
TRANSFORM	R
CONTROL 1	P
CONTROL 2	N
ARITHMETIC/LOGICAL UNIT	M
STATUS/MODE AND INTERRUPT	L
I/O AND TELETYPEWRITER/CONSOLE DISPLAY AND CLOCK	K
CARD READER AND LINE PRINTER††	J
STORAGE MODULE DRIVE OR CARTRIDGE DISK†††	H
MAGNETIC TAPE TRANSPORT (NRZI AND PHASE ENCODED)†††, †††††	G
8-CHANNEL COMMUNICATION LINE ADAPTER (6) OR DUAL-CHANNEL COMMUNICATION LINE ADAPTER††	F
TAPE CASSETTE††	E
IOM †††, †††††	D
OPEN††	C
OPEN†	B
FLEXIBLE DISK DRIVE†††	A
PAPER TAPE READER/PUNCH AND CARD PUNCH††, †††††	AA
MAGNETIC TAPE TRANSPORT (NRZI ONLY)††††	AB

† OPTIONAL PRINTED WIRING ASSEMBLY OR MODULE
†† OPTIONAL A/Q SLOT
††† OPTIONAL A/Q AND DMA SLOT
†††† OPTIONAL SET/SAMPLE SLOT
††††† FUTURE PRODUCT

Figure 1-4. Standard Chassis Layout (Printed Wiring Assembly Placement)

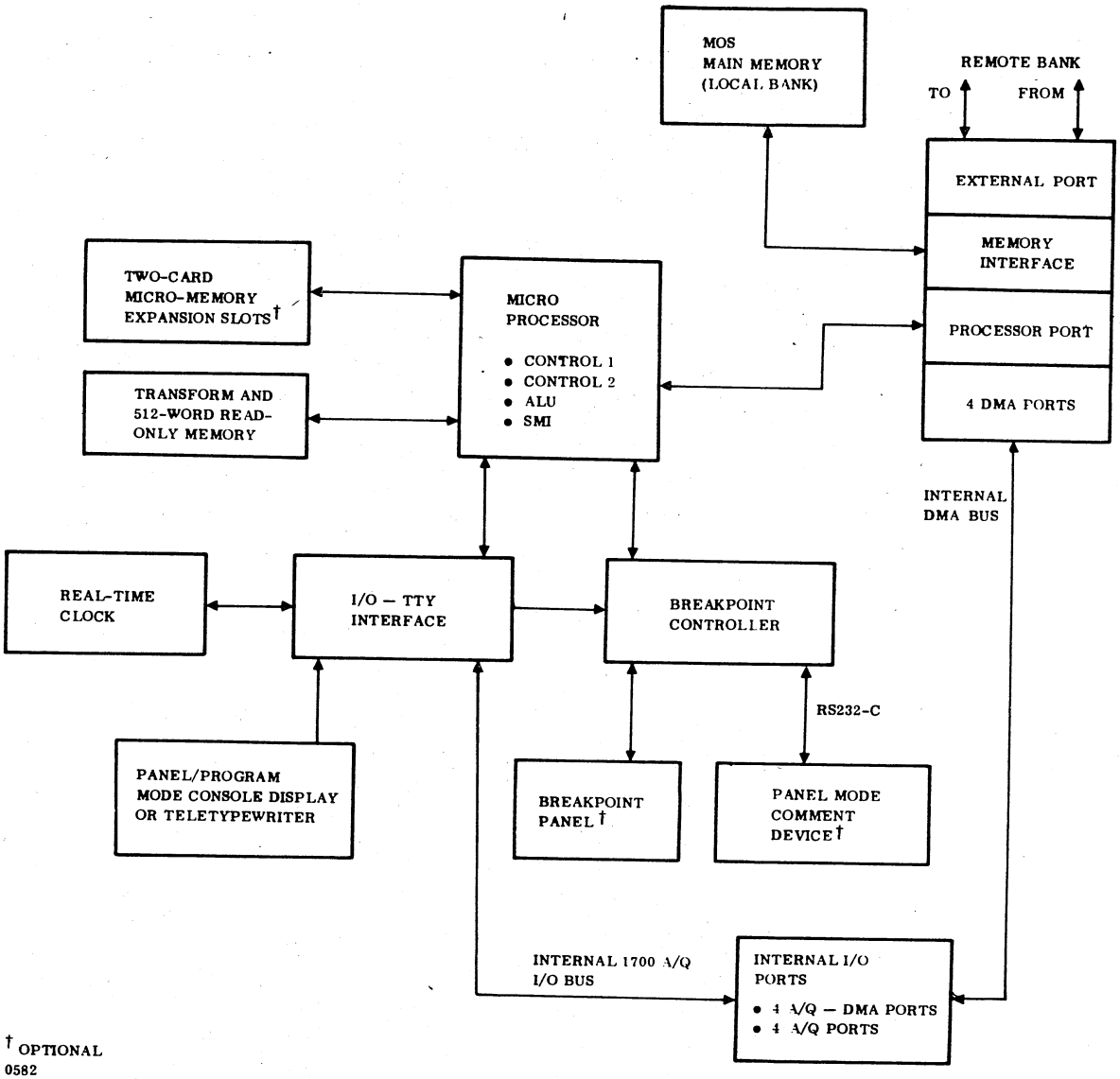


Figure 1-5. Processor Functional Block Diagram

The micro-programmable processor emulates a CDC 1700 computer system. It can perform all 1700 functions, utilizing an expanded instruction set with interfacing capabilities to 1700 Series peripherals. Figure 2-1 shows a block diagram of the processor system. The basic processor configuration includes the micro processor, main memory, input/output interface, and operator's interface. The flexible design of the system permits the user to incorporate his own equipment or to upgrade the processor with additional micro memory, the input/output capability, or a special hardware algorithm module.

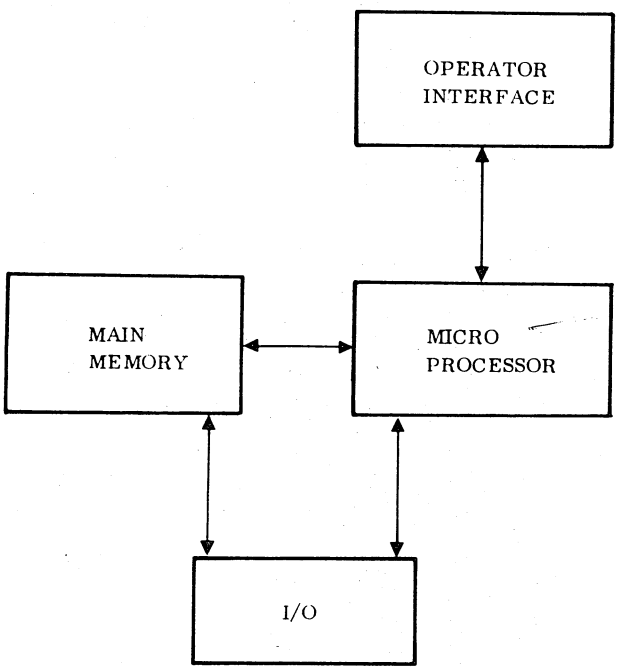


Figure 2-1. System Block Diagram

MICRO PROCESSOR

The central processing unit (CPU) is a special configuration that consists of an arithemtic logical unit (ALU) module, a status mode interrupt (SMI) module, two control modules, and the standard processor transform module. Detailed processor organization is shown in figure 2-2. This diagram shows processor registers interconnected primarily by sectors. A sector is a multiplexer that transfers one of several inputs to an output. They are either one, eight, 12 16, or 32 bits wide.

TRANSFORM AND TRANSFORM MODULE

Transforms enable quick and efficient decoding of an emulated instruction. A transform can be designed to extract bits from a register or registers, shift the bits to the required position, and add a base address or constant bits. This result can then be transferred to the micro-memory address register (transform jump) or to the K or N register (transform register load). For example, when a 1700 instruction is read from main memory, one micro-instruction transform jump transfers control to one of 108 micro-memory locations. Without the transform features, the above operation requires many micro instructions.

The transform hardware is packaged in a separate module and is implemented using three selectors. The transform module includes 1,024 micro instructions (512 words) in read-only memory. The majority of these instructions are used to execute the 1700 emulator. The read-only memory also contains instructions for the panel interface simulation via the I/O-TTY printed wiring assembly.

ALU AND DATA TRANSFER ORGANIZATION

The arithmetic logical unit provides the arithmetic and logical capabilities of the processor. This unit combines two input words of the system word length. These two inputs are combined according to the function code specified in the micro instruction. The result is immediately available at the output of the arithmetic logical unit for possible shifting via selector S3 and delivery to the destination register, memory interface, panel interface, and input/output. The unshifted output of the arithmetic logical unit is delivered to the SM and mask registers. The arithmetic logical unit operation regarding sign, zero, and magnitude (by means of carryout test) are available to the test bit logic for instruction sequencing.

The data transfer organization of the processor provides for storing data in one of six working registers and two files and for selecting data for processing through the arithmetic logical unit. Arithmetic logical unit results are transferred back to one of the registers or out of the organization to control external equipment.

The primary data registers are I, P, A, F, X, and Q.

The following are brief descriptions of the primary registers. Table 3-3 contains a comparison of the processor registers with 1700 registers.

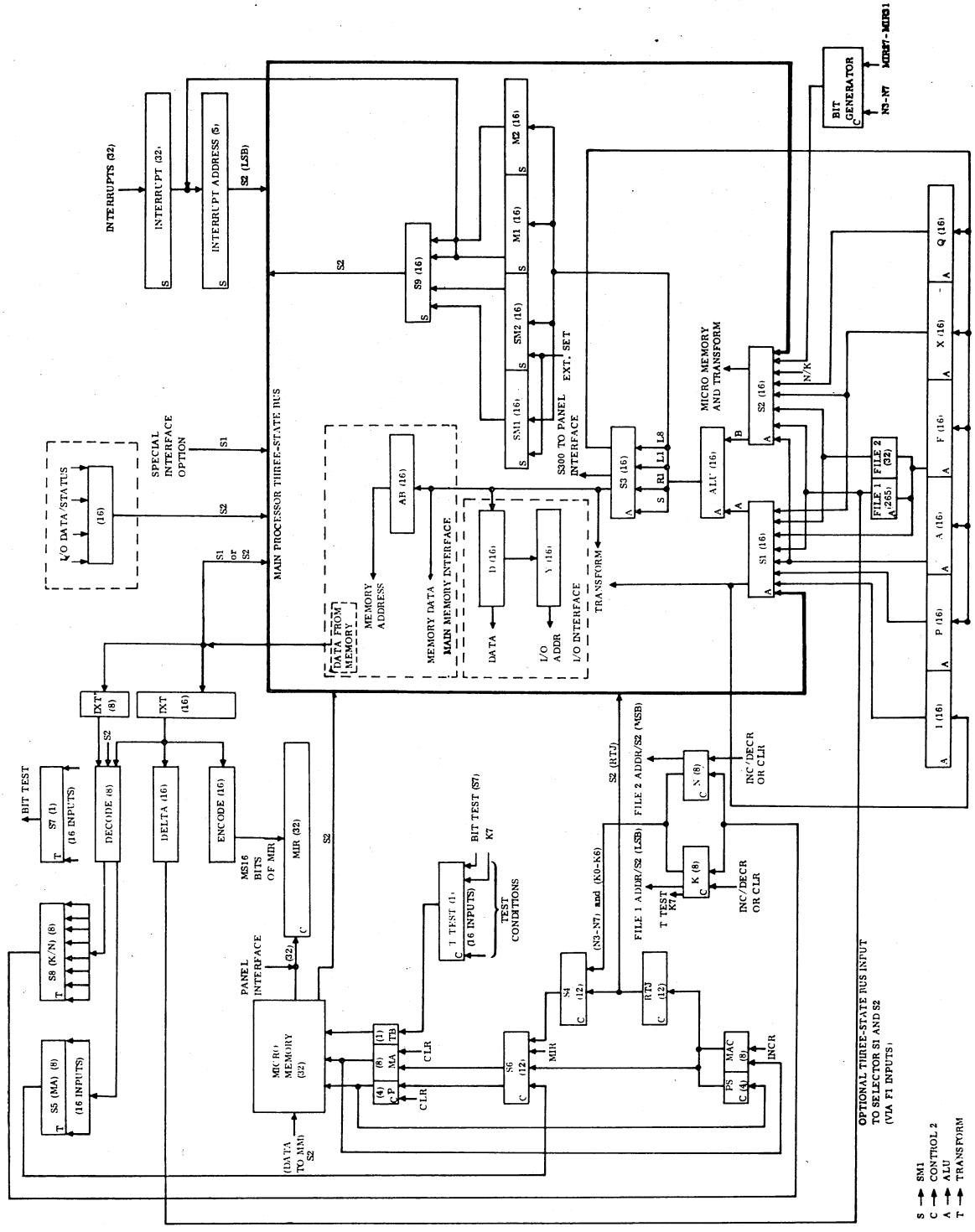


Figure 2-2. Detailed Block Diagram of Enhanced Processor

- I Register – A word-length register whose only input and output is the selector S1. This register should not be confused with the 1700 I register (location $00FF_{16}$).

- P Register† – A word-length, general-purpose register that receives data from the arithmetic logical unit and provides output to S1. Normally it is used to hold the software instruction counter.

- A Register† – A word-length, general-purpose register that receives data from the arithmetic logical unit and provides output to S1. The A register is mechanized as a shifting register and can be shifted left or right without using the arithmetic logical unit. The A register may also be combined with the Q register to form a double-length shifting register that operates independently of the arithmetic logical unit.

- F Register – A word-length, general-purpose register that receives data from the arithmetic logical unit and provides data to S1 or S2 as arithmetic logical unit input. This register is also used as the file entry register and contains information written into the files when they are used as the destination of an arithmetic logical unit operation.

- X Register – A word-length, general-purpose register that receives data from the arithmetic logical unit and provides data to S1 or S2.

- Q Register† – A word-length, general-purpose register that receives data from the arithmetic logical unit and provides output to S2. The Q register is mechanized as a shifting register. It may be shifted left or right in conjunction with the A register without using the arithmetic logical unit.

Other major portions of the standard processor are:

- File 2 – A 32-word scratchpad file that may be used as a general-purpose, word-sized register. It delivers its output to S1 and S2; data input is provided by the F register. File 2 is reserved for the emulator, except for registers R1, R2, R3, and R4, which are available to the 1700 programmer through enhanced instructions.

- Bit Generator (BG) – The BG circuit generates one bit at any position in a word as input to the B side of the arithmetic logical unit. Control to drive the bit generator is derived from either the micro instruction (bits 27 to 31) or the lower five bits of the N register. Control is usually obtained from the micro instruction. A bit setting in an SM register determines the input that drives the bit generator.

- Status/Mode Register (SM) – The SM register allows the micro program to control the mode of operation and also allows the micro program to examine the status of certain internal and external conditions. The processor can access one of two SM registers, SM1 and SM2.

The SM register module contains 16 bits of SM1 and 16 bits of SM2. All 32 bits of an SM module can be set or reset by the micro program by transferring information to the SM register from the output of the arithmetic logical unit. Master clear also clears SM1 and SM2.

- Interrupts and Mask Register – The interrupt system is implemented as a sampled data system at the micro-program level, instead of a true vectored interrupt system as used in conventional computers.

The mask register enables the processor to disable/enable interrupts. The processor can access two mask registers, M1 or M2. For each mask bit there is a corresponding bit in the interrupt register.

M1 is available to the 1700 programmer through the DMI instruction, while M2 (referred to as M) is available through the basic inter-register instruction (see section 4).

Interrupts are identified by their corresponding mask bits, which are assigned to control the interrupt recognition. The bits in the mask registers are identified as follows:

-Maks Register 1 (M1): M100 through M115

-Mask Register 2 (M2): M200 through M215

Interrupt addresses are generated by the interrupt address encoder, according to the assignments given in table 2-1.

The interrupt priorities correspond to the interrupt address generated; that is, interrupt address 00 is associated with the highest priority interrupt line and interrupt address 31 is associated with the lowest priority interrupt line. For example, an interrupt associated with M112 has priority over an interrupt associated with M111, and an interrupt address of 3 is developed by the interrupt address encoder.

- K Register – An 8-bit counter that may be cleared, incremented, or decremented. It is used to address file 1 in addition to any program usage as a counter.

- N Register – An 8-bit counter that may be cleared, incremented, or decremented. It is used to address file 2, control shifts, control the scale operations, and may be used as an iteration counter that controls micro-instruction execution.

- N/K Register – The N and K registers may be combined to provide operand addresses outside the current operating micro page.

- File 1 – An optional file of 256 general-purpose, word-sized registers that are addressed by the contents of the K register. The output of the addressed file is delivered to S1 and S2 and thus to the A and B side of the

†Available to the 1700 programmer.

TABLE 2-1. MASK REGISTER/INTERRUPT ADDRESSES

Mask Bit	Interrupt Address Mask Register 1	
M100	15	Lowest Priority (M1)
M101	14	
M102	13	
M103	12	
M104	11	
M105	10	
M106	09	
M107	08	
M108	07	
M109	06	
M110	05	
M111	04	
M112	03	
M113	02	
M114	01	
M115	00	Highest Priority (M1)
	Interrupt Address Mask Register 2	
M200	31	Lowest Priority (M2)
M201	30	
M202	29	
M203	28	
M204	27	
M205	26	
M206	25	
M207	24	
M208	23	
M209	22	
M210	21	
M211	20	
M212	19	
M213	18	
M214	17	
M215	16	Highest Priority (M2)

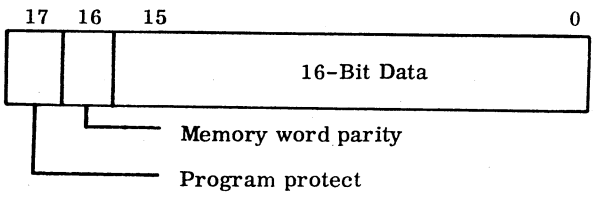
Note: The interrupt address generated is the same as its priority level; i.e., the highest priority interrupt generates a 0 interrupt address and the lowest priority interrupt generates a 31 interrupt address.

arithmetic logical unit on demand. This file 1 input to selectors S1 and S2 is a submultiplexed input to the arithmetic logical unit. Thus, depending on the state of status mode bit (SM111), either file 1 or transform data can be selected as either an A or B input to the arithmetic logical unit.

MAIN MEMORY

Main memory for the processor consists of 16K or 32K MOS semiconductor memory array modules, a data interface module, and an address and control interface module. The two interface modules provide the control and interfacing requireed for the processor/memory function and peripheral (DMA) equipment/memory functions.

The MOS memory words are in 18-bit format:



The parity and program protect bits are generated and tested in the interface modules. One set of interface modules can handle up to four 32K MOS memory array modules for a total of 131K words in the main processor chassis. In addition, an external memory bank, located in a second processor chassis, may be accessed by the processor for a total of 262K words of addressable memory.

If the error checking and correction option is installed, an additional 5 bits per word are stored. These ECC bits are stored on a separate memory array module. With ECC, memory is limited to 98K words in the main processor chassis.

The minimum processor memory cycle time is 600 nanoseconds, which is defined as the shortest possible time between successive read operations in main memory. The minimum processor main memory cycle time is 700 nanoseconds for write operations.

MAIN MEMORY CONFIGURATION

The main memory configuration is shown in figure 2-3.

The MOS memory configuration (for 16K to 131K) is a one-bank, three-port memory. One bank signifies that only one reference may take place at one time. Three ports provide

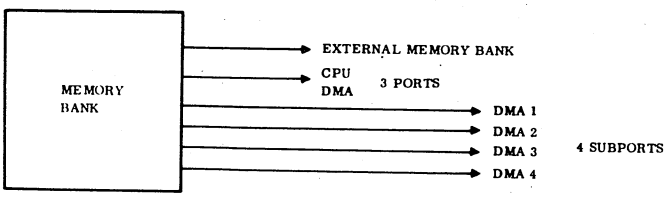


Figure 2-3. Main Memory Configuration

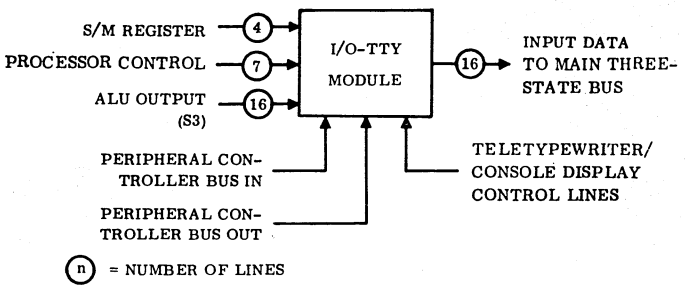
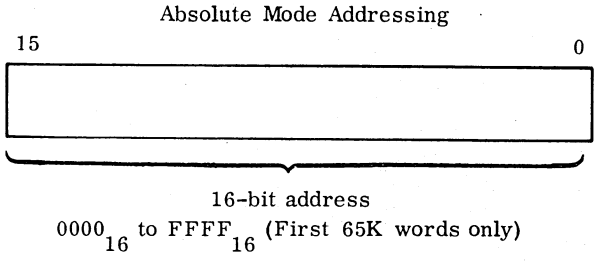
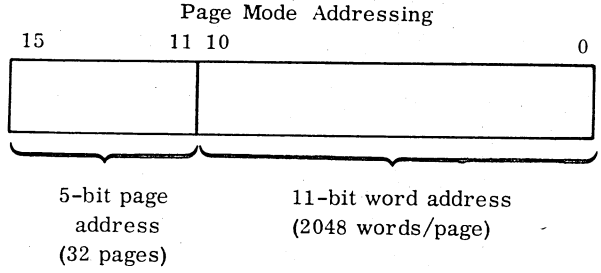


Figure 2-4. Major I/O-TTY Signal Flow Paths

three independent data and control paths to the memory; any port may request memory independent of any operation underway on the other ports. The ports are CPU, DMA (direct memory access), and the external memory bank port.

Main memory is addressed in 16-bit format, as shown in the following. Only the first 65K words are addressable in absolute mode. In page mode, all 131K words of MOS memory in the main processor chassis plus all 131K words of the external bank are addressable.





I/O-TTY MODULE

Figure 2-4 illustrates major signal flow paths to and from the I/O-TTY module.

This module includes the following components:

- Real-time clock – In conjunction with the micro code, it appears as a 1700 peripheral to the macro-level programmer.
- I/O teletypewriter/display control – This controller is an integral part of the module. It interfaces to Teletype Corporation ASR/KSR 33/35 Teletypes and to the CONTROL DATA RS232-C compatible conversational display terminals.
- Internal peripheral controller bus – Provides all input/output data lines, interrupts, and control signals necessary to generate, in conjunction with the micro code, an internal CDC 1700 A/Q (input/output) bus. This TTL-level bus is intended to interface with controllers located in the basic processor chassis.
- Panel interface simulation – A logic section that is required when a panel/program device is used for operator input in the panel mode.

The processor is interfaced to the input/output module as follows:

- ALU output – All output data and address information is provided from the output of the arithmetic logical unit via S3.
- SM register – All commands to peripheral controllers are generated by micro code manipulation of the processor status mode register.
- Processor control – Timing and control information for controlling internal input/output module data gating is provided from the processor control signals.
- Interrupts – Interrupts from peripheral controllers (within the basic chassis) are wired directly from the peripheral controller module to the processor.
- Input data and peripheral response signals – All of these are provided to the processor on the main processor three-state bus.
- Real-time clock – An integral part of the input/output module, the real-time clock appears as a 1700 peripheral to the macro-level software. Two functions are available to the macro-level program: enable limit interrupt and disable limit interrupt. Two status bits are also available to the macro-level program: limit interrupt and lost count.

The user may use his own design for input/output interfacing to facilitate use of special hardware.

BREAKPOINT PANEL/ BREAKPOINT CONTROLLER

The breakpoint controller is an optional circuit module available for manual interface to the processor. The controller provides interfaces for a breakpoint panel or for an RS232-C compatible console that has full-duplex serial ASCII characteristics. A slot is prewired in the processor chassis for the breakpoint controller. Control and data lines tie directly into the control logic of the controller and to the arithmetic logical unit printed wiring assembly within the processor.

This section discusses the operating procedure for the processor in general terms. Since each user has a different equipment application and setup, it is recommended that the user evaluate and develop his own operating procedure. The following sections present a general outline for startup and shutdown actions. Included is a description of the normal operator's interface to the processor.

STARTUP

The following startup sequence is a suggested outline:

1. Power-on switch. Turn the processor power-on switch to the ON position.
2. Peripherial power on sequence. Turn on all peripherals and auxiliary power units.

EMULATOR OR MACRO-PROGRAM DEADSTART

1. Master clear the machine.
2. Place the emulator or macro-program deadstart deck in the deadstart load device.
3. Make certain that no other deadstart devices are in the ready state.
4. Press the DEADSTART switch.

SHUTDOWN

De-energize all peripherals. Position the power-on switch to the OFF position.

SYSTEM FAILURE

After a system failure, follow the startup procedure and deadstart/autoload for restart.

MSOS AUTOLOAD

1. Master clear.
2. Press the autoload button for the mass storage controller.
3. Press ESCAPE on the panel/program device.
4. Type K31002800: $\leq$ 32K words memory

   Type K31000800: > 32K words memory
5. Type I @ .
6. After the initial MSOS messages, press ESCAPE on the panel/program device.
7. Set the program protect by typing J28 @.
8. Input data/time on the panel program device and continue.

OPERATOR INTERFACE

The normal system configuration includes a console display as the panel program device. The panel program device is connected to the processor through the I/O-TTY printed wiring assembly. It functions as a panel interface or a program (input/output) device.

FUNCTION CONTROL REGISTER

The function control register (FCR) (table 3-1) is the basic means of communication between the processor and the panel program device in the panel interface mode. The eight hexadecimal digits (32 bits) of the FCR can be grouped as follows (0 is highest order);

Display:	Digits 0 and 1
Machine Modes:	Digits 2 to 5
Machine Status:	Digits 6, 7

The display digits determine which individual registers of two groups of registers (identified in table 3-2) can be displayed and/or modified. Digits 2 to 5 of the FCR are used to set such conditions as selective stop on/off, step/run mode, etc.

The two least significant digits (6, 7) of the FCR are set by the processor and indicate the machine status, such as overflow on/off, macro storage parity error, protect fault, etc.

NOTES

1. Bits 14_{16} and 15_{16} of the FCR (enable console echo and enable auto-display) are mutually exclusive; that is, the operator may select one or the other, but not both simultaneously.
2. Digit 3 of the FCR (bits $0C_{16}$ to $0F_{16}$), breakpoint, is applicable only if the user has the optional breakpoint panel and breakpoint controller.

TABLE 3-1. FUNCTION CONTROL REGISTER (FCR)

Bit		Digit	Bit Definition
(LSB) 31	1F	7	Overflow
30	1E		Not Protected Instruction
29	1D		Protect Fault
28	1C		Parity Error
27	1B	6	Interrupt System Active
26	1A		Auto-Restart Enabled
25	19		Micro Running
24	18		Macro Running
23	17	5	Not used
22	16		Not used
21	15		Enable Auto Display
20	14		Enable Console Echo
19	13	4	Enable Micro Memory Write
18	12		Multilevel Indirect Addressing Mode
17	11		Not used
16	10		Suppress Console Transmit
15	0F	3	0 0 Breakpoint Off
14	0E		0 1 Instruction Reference BP
			1 0 Storage Operand BP
			1 1 All References BP
13	0D		Breakpoint Interrupt (Breakpoint Stop if Clear)
12	0C		Micro Breakpoint, Step, Go, Stop (Macro if Clear)
11	0B	2	Step
10	0A		Selective Stop
09	09		Selective Skip
08	08		Protect Switch
07	07	1	DISPLAY 1
06	06		
05	05		
04	04		
03	03	0	DISPLAY 0
02	02		
01	01		
(MSB) 00	00		

Status Only

TABLE 3-2. DISPLAY CODE DEFINITIONS

Code		Display 1	Display 0
0	0 0 0 0	FCR	F2 (Addressed by N)
1	0 0 0 1	P†	N (MSBs)††
2	0 0 1 0	I	K (LSBs)††
3	0 0 1 1		X
4	0 1 0 0	A†	Q
5	0 1 0 1	MIR	F
6	0 1 1 0	BP/P-MA (Display Only)	F1 { Addressed by K / Enabled by SM111
7	0 1 1 1	P-MA (Display Only)	MEM
8	1 0 0 0	SM1	
9	1 0 0 1	M1	$\overline{\text{RTJ}}$
A	1 0 1 0	SM2	
B	1 0 1 1	M2	
C	1 1 0 0		MM
D	1 1 0 1	A*	
E	1 1 1 0	X*	
F	1 1 1 1	Q*	

† Used to address main memory. Automatically incremented after each memory reference.

†† The combined contents of these two registers are used to address micro memory. The K register is automatically incremented after each memory reference. The N register does not automatically increment.

3. Unassigned display codes (table 3-2) should be assumed to be undefined.

4. Selecting BP or P-MA (table 3-2) results in both BP and P-MA being displayed. BP is the leftmost 16 bits and P-MA is the rightmost 16 bits. BP can be modified only if BP is selected; P-MA cannot be modified in either case.

5. Selecting N or K (table 3-2) results in both N and K being displayed. N is the left eight bits and K is the right eight bits. However, when N is selected, only the N register can be modified; when K is selected, only the K register can be modified.

AUTO-DISPLAY

When auto-display is enabled, the register selected by the control code and display code is output to the operator's interface and continuously updated (assuming the operator's interface contains a console display and not a teletype-writer). With auto-display enabled, pressing a terminator (:, G, or @) with no characters preceding it causes a go signal.

PANEL INTERFACE CONTROL COMMANDS

The control commands used in the panel interface mode include: H, I, J, K, L, @ , :, G, and ?. Control commands H through L identify the type of data or operation entered or returned. The at symbol (@), the colon (:), and G all perform an entry termination function. The @ also causes the operator's interface to go from the panel interface mode to program (A/Q) mode. The question mark, ?, generates a master clear.

A normal entry consists of one control character H through L; two, four, or eight hexadecimal digits 0 through F; and a terminating entry (: or G), in that order.

A normal response consists of the control character identifying the data that follows and four or eight hexadecimal digits. If a transmission or operator error occurs on the entry, an asterisk (*) precedes the control character and the function control register is unconditionally displayed with the last legal control character. All entries except the ? cause a response, unless bit 10_{16} (suppress console transmit) of the FCR is set. The following are examples of the control functions. The colon (:) is used as the terminating entry.

- Master clear – A master clear can be generated in several ways:

  -A power on master clear

  -The master clear button on the breakpoint panel

  -A signal from a peripheral controller

  -A question mark from a panel device (programmers console)

  NOTE

  Baud rate compatibility between the panel device and the machine must exist for ? master clear.

- Stop/go control – The following entry causes a go:

  I: (Initiate)

This is a micro go if bit 12 of the FCR is set. It is both a micro and macro go if bit 12 of the FCR is clear.

The I control function may also be used to set a bit in the FCR.

The following entry causes a stop:

H: (Halt)

This is a micro stop if bit 12 of the FCR is set. It is a macro stop if bit 12 of the FCR is clear.

The response to a start or stop entry is a display of the FCR.

The H control function may also be used to clear a specific bit in the FCR. The entry

H14

clears bit 14_{16} in the FCR and the response is a display of the updated FCR.

NOTE

The clear and set capabilities of the H and I control functions are not available in the panel simulation mode.

- J control function – The J control function is used to replace the contents of the function control register in a digit mode. While it may be used to change the value of any FCR digit, it is generally used to change digits 0 and 1. The value of Display 0 and Display 1 specifies which processor parameter is displayed on display requests or entered on enter requests (refer to table 3-3). J functions always consist of J followed by two hexadecimal digits and a terminator (:, G, or @). The first hexadecimal digit specifies the FCR digit 0 through 5 and the second hexadecimal digit specifies the value the digit is to assume, 0 through F.

  The function code:

  J14:

  sets FCR digit 1 to 4 (select the A register), and the response is a display of the updated FCR.

  The J code is also used to alternately display the upper and lower 16 bits of a 32-bit register on the 16-bit breakpoint panel display.

  In the panel simulation mode, J: results in the display of the entire FCR register. There is no upper/lower mode.

- K control function – The K control function is used to display or enter data into the parameter specified by Display 1. The K function uses two formats. The first format is a request to display the parameter specified by Display 1:

  K:

TABLE 3-3. PROCESSOR/1700 REGISTER CORRESPONDENCE

Processor	1700
P	P
A	A
Q	Q
X	(P) (i.e., next instruction) (display only)
I	I (see notes 1 and 2) (display only)
F2(1)	R1
F2(2)	R2
F2(3)	R3
F2(4)	R4
F2(5)	Q (display only)
F2(6)	A (display only)
F2(7)	I (see notes 1 and 2)
M2	M
NOTE: To change I: 1. Change location $00FF_{16}$ 2. Change F2(7)	

The second format is an enter data request. The data is entered into the parameter specified by Display 1. It consists of K followed by four or eight hexadecimal digits, followed by a terminator (:, G, or @). The hexadecimal digits are the data to be entered. For example:

-To display the P register, type:

J11: Set Display 1 to P register (FCR Digit 1 = 1_{16}).

K: Display parameter selected in Display 1.

-To enter $14FE_{16}$ into the breakpoint register, type:

J16: Set Display 1 to BP register (FCR Digit 1 = 6_{16}).

K14FE: Enter data into the parameter selected in Display 1.

- L control function – The L function is operationally the same as the K function, except that it is associated with Display 0.

NOTE

When main memory is displayed or entered, the register selected in Display 1 is the main memory address. The Display 1 selection must be the P or A register. This register is incremented by 1 after the display. In the panel simulation mode, the Display 1 section must be in the P register. When micro memory is displayed or entered, the K register is the eight least significant bits of the address, and the N register provides the remaining bits. The K register is incremented by 1 after the display.

- Breakpoint (BP) – There are two types of breakpoint: micro and macro. If bit 12 of the FCR is set, micro breakpoint is selected. If bit 12 is clear, macro breakpoint is selected. In the panel simulation mode there is no micro or macro breakpoint capability.

Bits 14 and 15 of the FCR are used to select three types of macro breakpoint:

Bit 14	Bit 15	
0	0	Breakpoint not selected
0	1	Instruction reference breakpoint
1	0	Store operand breakpoint
1	1	All references breakpoint

A macro breakpoint occurs if the breakpoint register is equal to the macro memory address and the select conditions are met. For example:

J16: Set display 1 to the breakpoint register.

K0050: Set the breakpoint register to 0050_{16}.

J31: Set macro mode and breakpoint on the instruction reference.

A stop occurs after the instruction at macro location 50_{16} is executed.

If bit 13 of the FCR is set, an interrupt occurs when the breakpoint conditions are met rather than a stop.

For a micro breakpoint, P-MA is compared to the lower 12 bits of the breakpoint register. In addition, the upper/lower selection (32-bit select) is compared to bit 13 of the breakpoint register. If all bits are equal and the combination of FCR bits 14 and 15 is not zero, then a micro stop occurs. If FCR bit 14 is set, then a comparison of FCR bit 13 and the upper/lower selector is not required.

- Auto-display - When auto-display is enabled, the register selected by the control and display codes is output to the operator's interface and continuously updated as long as the interface is a display terminal and not a teletypewriter. Depressing a terminator (:, G, or @) with no characters preceding it causes a go signal, which is useful for stepping through a micro or macro program.

NOTE

Auto-display mode and echo mode should never be selected simultaneously. In other words, FCR bits 20 and 21 should be mutually exclusive.

PANEL/PROGRAM MODE COMMANDS

Commands for use in the program mode are escape (ESC) and manual interrupt. The ESC command causes the panel/program device to go from program mode to panel interface mode. It sets the reserve status line, which indicates to the software that the panel/program device is busy if the macro program attempts to reference it.

The manual interrupt is generated by a control G (BELL) command. It is used instead of a console manual interrupt button.

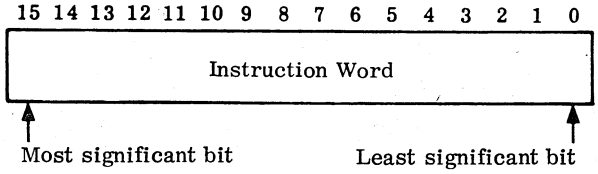
The command for use in panel mode is the @ symbol. It generates a release reserve as it causes the panel/program device to enter into the program mode from the panel mode. Selecting the @ during program mode is accepted as a normal ASCII character with no special function.

I/O OPERATIONS

With the exceptions specified in the program mode commands, the program mode is to be used as standard operator data interface to the processor for input/output.

INSTRUCTION FORMAT

The processor instruction word shown in the following example consists of 16 bits, numbered right to left as 0 to 15, with the leftmost bit, 15, being the most significant and the rightmost bit, 0, being the least significant.



Hexadecimal (base 16) notation is used in this computer.

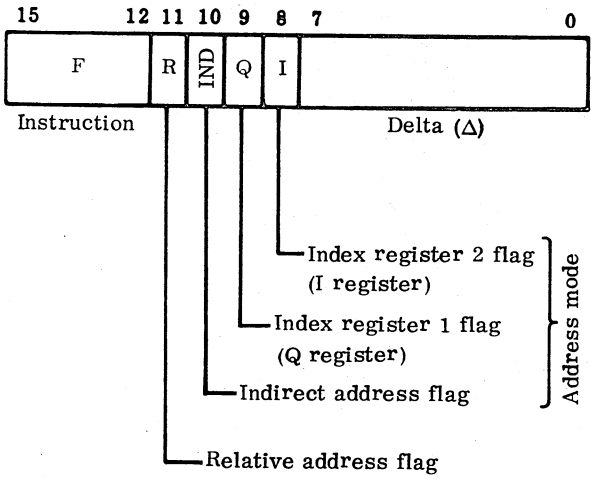
The processor is composed of a basic and an enhanced instruction set. The basic set is 1700-compatible and is divided into storage reference, register reference, inter-register, skip, and shift instructions. The enhanced instruction set is divided into the enhanced storage reference, field-reference, enhanced inter-register, enhanced skip, decrement and repeat, and miscellaneous instructions.

BASIC INSTRUCTION SET

STORAGE REFERENCE

The storage reference instructions shown in the following illustration contain three fields: instruction, address mode, and delta. The instruction field contains the operation code.

The address mode field contains flags for indexing, indirect addressing, and relative addressing. The delta field is a signed 8-bit address modifier in which the most significant bit is the sign bit. Storage reference instructions have the following format:



Five types of addresses and/or address methods are created by these instructions:

- Instruction address – The address of the instruction being executed; also called P
- Indirect address – A storage address that contains an address rather than an operand
- Base address – The operand address after all indirect addressing but before modification by the index registers. The base address is the effective address when no indexing is specified.
- Effective address – The final address of the operand. At certain times, the effective address equals the operand for read-operand type instructions (refer to table 4-1).
- Indexing – The processor has two index registors. Index register 1 is the Q register; index register 2 is storage location $00FF_{16}$ (1 register). The base address may be modified by either or both of the index registers. If the index 1 flag is set, the contents of the Q register are added to the base address to form the effective address. If the index register 2 flag is set, the contents of storage location $00FF_{16}$ (I register) are added to the base address to form the effective address. If both index register flags are set, the contents of Q are added to base address; then the contents of $00FF_{16}$ are added to the result to form the effective address. B (for both) is used for indexing both the Q and I register. Indexing occurs after completion of indirect addressing.

The processor uses the 16-bit ones complement adder during indexing operations. Consequently, the index register contents are treated as signed quantities (bit 15 is the sign bit).

The storage reference instructions (refer to table 4-1) have eight different types of addressing modes: 8-bit absolute, 8-bit absolute indirect, 8-bit relative, 8-bit relative indirect, absolute constant, 16-bit storage, 16-bit relative, and 16-bit relative indirect.

- 8-bit absolute (address mode bits = 0, 1, 2, or 3) – Both relative and indirect flags are set to 0 and delta is not set to 0. The base address equals delta. Delta has no sign bit. The contents of the index registers, when specified, are added to the base address to form the effective address.
- 8-bit absolute indirect (address mode bits = 4, 5, 6, or 7) – The relative address flag is set to 0, the indirect flag is set to 1, and delta is not set to 0. The 8-bit value of delta is an indirect address. Delta is a magnitude quantity for this operation (no sign bit).
- 8-bit relative (address mode bits = 8, 9, A, or B) – The relative flag is set to 0, and delta is not set to 0. The base address is equal to the instruction address P plus the value of delta with sign extended. The contents of the index registers, when specified, are added to the base address to form the effective address.

TABLE 4-1. STORAGE REFERENCE INSTRUCTION ADDRESSING

Mode	Binary 11 10 9 8	Hex.	Δ Delta	Effective Address	Address of Next Instruction
8-Bit Absolute	0000	0	≠0	Δ	P+1
	0001	1		Δ+(00FF)	
	0010	2		Δ+(Q)	
	0011	3		Δ+(Q)+(00FF)	
8-Bit Absolute Indirect††	0100	4		(Δ)	
	0101	5		(Δ)+(00FF)	
	0110	6		(Δ)+(Q)	
	0111	7		(Δ)+(Q)+(00FF)	
8-Bit Relative	1000	8		P+Δ	
	1001	9		P+Δ+(00FF)	
	1010	A		P+Δ+(Q)	
	1011	B		P+Δ+(Q)+(00FF)	
8-Bit Relative Indirect††	1100	C		(P+Δ)	
	1101	D		(P+Δ)+(00FF)	
	1110	E		(P+Δ)+(Q)	
	1111	F		(P+Δ)+(Q)+(00FF)	
Absolute Constant	0000	0	=0	P+1	P+2
	0001	1		(P+1)+(00FF)†	
	0010	2		(P+1)+(Q)†	
	0011	3		(P+1)+(Q)+(00FF)†	
16-Bit Storage††	0100	4		(P+1)	
	0101	5		(P+1)+(00FF)	
	0110	6		(P+1)+(Q)	
	0111	7		(P+1)+(Q)+(00FF)	
16-Bit Relative	1000	8		P+1+(P+1)	
	1001	9		P+1+(P+1)+(00FF)	
	1010	A		P+1+(P+1)+(Q)	
	1011	B		P+1+(P+1)+(Q)+(00FF)	
16-Bit Relative Indirect††	1100	C		(P+1+(P+1))	
	1101	D		(P+1+(P+1))+(00FF)	
	1110	E		(P+1(P+1))+(Q)	
	1111	F		(P+1+(P+1))+(Q)+(00FF)	

†Effective address is the operand for read-operand type instructions.

††Multilevel only in 32K mode

- 8-bit relative indirect (address mode bits = C, D, E, or F) – Both relative and indirect flags are set to 1. If delta is not set to 0, the value of the instruction address P plus the value of delta with sign extended is an indirect address. If bit 15 of the contents of this indirect address is 0, the contents of this indirect address is the base address. If bit 15 of the contents of the indirect address is set when the computer is in 32K mode, another indirect address is indicated.

- Absolute constant (address mode bits = 0, 1, 2, or 3) – Both relative and indirect flags and delta are set to 0.

  When the address mode bits are set to 0, P + 1 is the effective address. When the address mode bits are set to 1, 2, or 3, the contents of P + 1 plus the contents of one or both index registers form the effective address. The effective address is taken as the operand for read-operand type instructions.

- 16-bit storage (address mode bits = 4, 5, 6, or 7) – The relative address flag and delta are set to 0 and the indirect flag is set to 1. The contents of location P + 1 is an indirect address. When the base address is formed (indirect addressing complete), the contents of one or both index registers, if specified, are added to form the effective address.

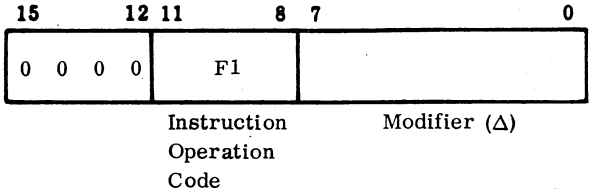
- 16-bit relative (address mode bits = 8, 9, A, or B) – The relative address flag is set to 1, and the indirect address flag and delta are set to 0. If no indexing is specified, the instruction address P + 1 plus the contents of location P + 1 form the base address or effective address. If indexing is specified, the contents of the specified index registers are added to the base address to form the effective address.

- 16-bit relative indirect (address mode bits = C, D, E, or F) – Both relative and indirect flags are set to 1. In 65K mode, the contents of P + 1 + (P + 1)† is the base address. Then the contents of the index registers, when specified, are added to the base address to form the effective address. In 32K mode, P + 1 + (P + 1) equals the base address if bit 15 of (P + 1) is 0; if 1, then P + 1 + (P + 1) forms an indirect address. This process continues until bit 15 equals 0.

Table 4-2 shows all the addressing possibilities for storage reference instructions that may be obtained through combinations of flag bits.

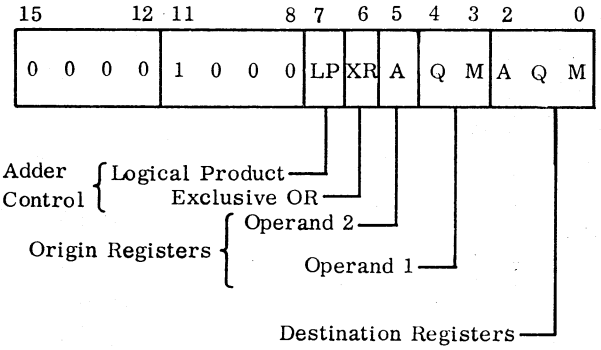
REGISTER REFERENCE

Register reference instructions (refer to table 4-3) use the address mode field for the operation code. These instructions are identified by 0s in the upper four bits of an instruction and the F1 instruction operation code (address mode field) cannot be a one, eight, or 15:



INTER-REGISTER

Inter-register instructions (F1 = 8) are identified by an 8 in the address mode field and a 0 in the instruction mode field. These instructions (table 4-4) cause data from certain combinations of origin registers to be sent through the adder to any combination of destination registers. Various operations, selected by the adder control lines, are performed on the data as it passes through the adder. The inter-register instruction format is:



The origin registers are considered as operands. There are two kinds:

- Operand 1 may be one of the following:

  $FFFF_{16}$ (bit 5 = 0)

  The contents of A (bit 5 = 1)

- Operand 2 may be one of the following:

  $FFFF_{16}$ (bit 4 = 0 and bit 3 = 0)

  The contents of M (bit 4 = 0 and bit 3= 1)

  The contents of Q (bit 4 = 1 and bit 3 = 0)

  The OR, bit-by-bit, of the contents of Q and M (bit 4 = 1 and bit 3 = 1)

†( ) Denotes contents of expression

TABLE 4-2. STORAGE REFERENCE INSTRUCTIONS

Instruction	Mnemonic	Description
Unconditional Jump F = 1	JMP	Effective address specifies the location of the next instruction
Multiply Integer F = 2	MUI	Multiply the contents of the storage location specified by the effective address in the A register. The 32-bit product replaces the contents of Q and A with the most significant bits in the Q register. Ones complement arithmetic is used.
Divide Integer F = 3	DVI	Divide the combined contents of the Q and A registers by the contents of the effective address. The Q register contains the most significant bits before execution. The quotient is in the A register and the remainder is in the Q register at the end of execution. The overflow indicator is set if the magnitude of the quotient is greater than the capacity of the A register. Once set, the overflow indicator remains set until a skip on overflow instruction is executed.
Store Q F = 4	STQ	Store the contents of the Q register in the storage location specified by the effective address. The contents of Q are not changed.
Return Jump F = 5	RTJ	Replace the contents of the storage location specified by the effective address with the address of the next consecutive instruction. The address stored in the effective address will be P + 1 or P + 2, depending on the addressing mode of RTJ. The contents of P are then replaced with the effective address + 1.
Store A F = 6	STA	Store the contents of the A register in the storage location specified by the effective address. The contents of A are not altered.
Store A, Parity to A F = 7	SPA	Store the contents of the A register in the storage location specified by the effective address. Set the A register to 0001_{16} if the parity bit of the word stored in the effective address is set. If the parity bit is not set, set the A register to 0000.
Add to A F = 8	ADD	Add the contents of the storage location specified by the effective address to the contents of the A register. Ones complement arithmetic is used. The overflow indicator will be set if the magnitude of the sum is greater than the capacity of the A register. Once set, the overflow indicator will remain set until a skip on overflow instruction is executed.
Subtract from A F = 9	SUB	Subtract the contents of the storage location specified by the effective address from the contents of the A register. Ones complement arithmetic is used. The overflow operation is the same as in ADD.

TABLE 4-2. STORAGE REFERENCE INSTRUCTIONS (Contd)

Instruction	Mnemonic	Description
And with A F = A	AND	Form the logical product, bit-by-bit, of the contents of the storage location specified by the effective address and the contents of the A register. The result replaces the contents of A.
Exclusive OR with A F = B	EOR	Form the logical difference (exclusive OR), bit-by-bit, of the contents of the storage location specified by the effective address and the contents of the A register. The results replace the contents of the A register.
Load A F = C	LDA	Load the A register with the contents of the storage location specified by the effective address. The contents of the storage location are not altered.
Replace Add One in Storage F = D	RAO	Add 1 to the contents of the storage location specified by the effective address. The contents of A and Q are not changed. Ones complement arithmetic is used. Operation on overflow is the same as in ADD.
Load Q F = E	LDQ	Load the Q register with the contents of the storage location specified by the effective address. The contents of the storage location are not altered.
Add to Q F = F	ADQ	Add the contents of the storage location specified by the effective address to the contents of the Q register. Ones complement arithmetic is used. Operation on overflow is the same as in ADD.

TABLE 4-3. REGISTER REFERENCE INSTRUCTIONS

Instruction	Mnemonic	Description
Selective Stop F1 = 0 Δ = 0	SLS	If this instruction is executed when the STOP switch is on, the machine is stopped. When the switch is off, the instruction becomes a pass.
Input to A F1 = 2	INP	Read one word from an external device into the A register. The word in the Q register selects the sending device. If the device sends a reply, the next instruction comes from P + 1. If the device sends a reject, the next instruction comes from P + 1 + Δ, where Δ is an eight-bit signed number including sign. An internal reject causes the next instruction to come from P + Δ.

TABLE 4-3. REGISTER REFERENCE INSTRUCTIONS (Contd)

Instruction	Mnemonic	Description
Output from A F1 = 3	OUT	Output one word from the A register to an external device. The word in the Q register selects the receiving device. If the device sends a reply, the next instruction comes from P + 1. If the device sends a reject, the next instruction comes from P + 1 + Δ, where Δ is an eight-bit signed number including sign. An internal reject causes the next instruction to come from P + Δ.
Increase A F1 = 9	INA	Replace the contents of A with the sum of the initial contents of A and delta. Delta is treated as a signed number with the sign extended into the upper eight bits. Operation on overflow is the same as in ADD.
Enter A F1 = A	ENA	Replace the contents of the A register with the eight-bit delta, sign extended.
No Operation F1 = B Δ = 0	NOP	
Enter Q F1 = C	ENQ	Replace the contents of Q with the eight-bit delta, sign extended.
Increase Q F1 = D	INQ	Replace the contents of Q with the sum of the initial contents of Q and delta. Delta is treated as a signed number with the sign extended into the upper eight bits. Operation on overflow is the same as in ADD.
Enable Interrupt† F1 = 4 Δ = 0	EIN	Activate the interrupt system. The interrupt system must be active and the mask bit set for an interrupt to be recognized.
Inhibit Interrupt† F1 = 5 Δ = 0	IIN	De-activate the interrupt system.
Set Program Protect† F1 = 6 Δ = 0	SPB	Set the program protect bit in the address specified by Q.

†These instructions are only legal when the PROGRAM PROTECT switch is off, or the instructions themselves are protected. If an instruction is illegal, it becomes a Selective Stop and an interrupt on Program Protect Fault is possible (if selected).

TABLE 4-3. REGISTER REFERENCE INSTRUCTIONS (Contd)

Instruction	Mnemonic	Description
Clear Program Protect† F1 = 7 Δ = 0	CPB	Clear the program protect bit in the address specified by Q.
Exit Interrupt State† F1 = E	EXI	Exit from an interrupt state specified by delta. This instruction reads the address containing the return address, resets the overflow indicator according to bit 16, activates the interrupt system, and jumps to the return address.

†These instructions are only legal when the PROGRAM PROTECT switch is off, or the instructions themselves are protected. If an instruction is illegal, it becomes a Selective Stop and an interrupt on Program Protect Fault is possible (if selected).

TABLE 4-4. INTER-REGISTER INSTRUCTIONS

Description	Mnemonics	Bit 7 6 5 4 3
Set to Ones	SET	1 0 0 0 0
Clear to Zero	CLP	0 1 0 0 0
Transfer A	TRA	1 0 1 0 0
Transfer Q	TRQ	1 0 0 1 0
Transfer Q or M	TRB	1 0 0 1 1
Transfer Complement A	TCA	0 1 1 0 0
Transfer Complement M	TCM	0 1 0 0 1
Transfer Complement Q	TCQ	0 1 0 1 0
Transfer Complement Q or M	TCB	0 1 0 1 1
Transfer Arithmetic Sum A, M	AAM	0 0 1 0 1
Transfer Arithmetic Sum A, Q, or M	AAB	0 0 1 1 1
Transfer Arithmetic Sum A, Q	AAQ	0 0 1 1 0
Transfer Exclusive OR A, M	EAM	0 1 1 0 1

TABLE 4-4. INTER-REGISTER INSTRUCTIONS (Contd)

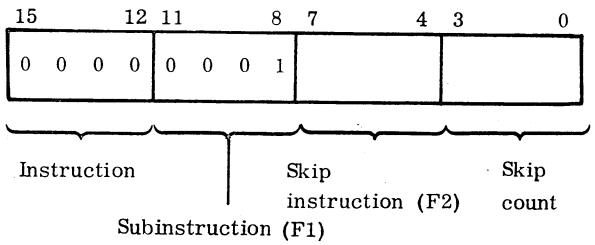
Description	Mnemonics	Bit 7 6 5 4 3
Transfer Exclusive OR A, Q	EAQ	0 1 1 1 0
Transfer Exclusive OR A, Q, or M	EAB	0 1 1 1 1
Transfer Logical Product A, M	LAM	1 0 1 0 1
Transfer Logical Product A, Q	LAQ	1 0 1 1 0
Transfer Logical Product A, Q, or M	LAB	1 0 1 1 1
Transfer Complement Logical Product A, M	CAM	1 1 1 0 1
Transfer Complement Logical Product A, Q	CAQ	1 1 1 1 0
Transfer Complement Logical Product A, Q, or M	CAB	1 1 1 1 1

The following operations are possible (refer to table 4-5 for examples of all possible four-bit operands):

- LP = 0 and XR = 0 – The data placed in the destination registers is the arithmetic sum of operand 1 and operand 2. The overflow indicator operates the same as in ADD.
- LP = 1 and XR = 0 – The data placed in the destination register is the logical product, bit-by-bit, of operand 1 and operand 2.
- LP = 0 and XR = 1 – The data placed in the destination registers is the exclusive OR, bit-by-bit, of operand 1 and operand 2.
- LP = 1 and XR = 1 – The data in the destination registers is the complement of the logical product, bit-by-bit, of operand 1 and operand 2.

SKIP

Skip instructions (F1 = 1) are identified by a 1 in the address mode field and a 0 in the instruction mode field:

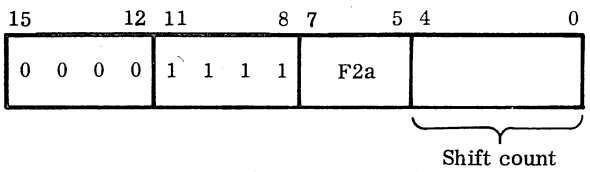


When the skip condition is met, the contents of the skip count + 1 is added to P to obtain the address of the next instruction (for example, when the skip count is 0, go to P + 1). When the skip condition is not met, the address of the next instruction is P + 1 (skip count ignored). The skip count does not have a sign bit.

The skip instruction are listed in table 4-6.

SHIFT

Shift instructions are identified by a 15 in the address mode field and a 0 in the instruction mode field. These instructions shift A or Q, or QA left or right for the number of places specified by the 5-bit shift count. The sign is extended on right shifts. Left shifts are end-around. This instruction has the following format:



The shift instructions (F2a) are listed in table 4-7.

ENHANCED MACRO INSTRUCTIONS

Instruction formats for enhancements to the 1700 instruction repertoire are upward-compatible with the existing 1700 computers. They make use of previously undefined instruction formats.

TABLE 4-5. INTER-REGISTER INSTRUCTION TRUTH TABLE

Operand 1	Operand 2	LP = 0 XR = 1	LP = 1 XR = 0	LP = 1 XR = 1	LP = 0 XR = 0
0	0	0	0	1	Arithmetic sum
0	1	1	0	1	
1	0	1	0	1	
1	1	0	1	0	

Notes:
1. Register transfers can be accomplished with LP = 0, XR = 0, and by making operand 1 or operand 2 equal to $FFFF_{16}$.
2. Without destroying either operand, magnitude comparisons can be done with LP = 0, XR = 0, no destination register selected, and by testing the overflow indicator.
3. Complementing registers can be done with LP = 0, XR = 1, and making operand 1 and operand 2 equal to $FFFF_{16}$.

TABLE 4-6. SKIP INSTRUCTIONS

Instruction	Mnemonic	Description
Skip if A = +0	SAZ	F2 = 0
Skip if A = +0	SAN	F2 = 1
Skip if A = +	SAP	F2 = 2
Skip if A = -	SAM	F2 = 3
Skip if Q = +0	SQZ	F2 = 4
Skip if Q = +0	SQN	F2 = 5
Skip if Q = +	SQP	F2 = 6
Skip if Q = -	SQM	F2 = 7
Skip if switch is set	SWS	F2 = 8
Skip if switch is not set	SWN	F2 = 9
Skip on overflow. SOV clears the overflow indicator.	SOV	F2 = A
Skip on no overflow	SNO	D2 = B
Skip on storage parity error. SPE clears the storage parity error signal and indicator.	SPE	F2 = C

TABLE 4-6. SKIP INSTRUCTIONS (Contd)

Instruction	Mnemonic	Description
Skip on no overflow	SNO	D2 = B
Skip on storage parity error. SPE clears the storage parity error signal and indicator.	SPE	F2 = C
Skip on no storage parity error	SNP	F2 = D
Skip on program protect fault†	SPF	F2 = E
Skip on no program protect fault†	SNF	F2 = F

†The program protect fault is set by:

1. An unprotected instruction attempting to write into a protected address
2. A protected instructed executed immediately following a unprotected instruction, except when an interrupt has caused the instruction sequence
3. Execution of any unprotected instruction that attempts to alter the interrupt sustem.

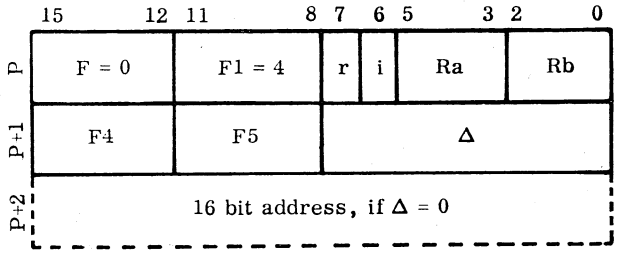
The program protect fault is cleared when an SPF or SNF is executed. The program protect fault cannot be set if the program protect system is disabled.

TABLE 4-7. SHIFT INSTRUCTIONS

Instruction Name	Mnemonic	Description
Q Right Shift	QRS	F2a = 1
A Right Shift	ARS	F2a = 2
Long Right Shift (QA)	LRS	F2a = 3
Q Left Shift	QLS	F2a = 5
A Left Shift	ALS	F2a = 6
Long Left Shift (QA)	LLS	F2a = 7

ENHANCED STORAGE REFERENCE

These instructions have the following format:



The enhanced storage reference instructions are identified when the F field is 0, the F1 field is equal to 4, and the r, i, Ra, and Rb fields are not all 0. (If these fields are all 0, the instruction is an EIN.) This instruction is made up of two (or three, if delta is 0) words.

The enhanced storage reference instructions are similar to the basic storage references in that they contain four parts: instruction field (F4), instruction mode field (F5), addressing mode fields (delta, r, i, and Ra), and register Rb. Two operands (A and B) are specified for executing the instruction.

The F4 field determines the instruction (e.g., add, subtract, etc.). The F5 field determines the instruction mode:

F5 = 0 Word processing; register destination

1 Word processing; memory destination

2 Character processing; register destination

3 Character processing; memory destination

NOTE

F5 is not used for subroutines jumps and subroutine exit. The register/memory destination bit F5 is not used for compare instructions (see below).

The addressing mode fields contain four fields:

1. Delta determines 8- or 16-bit addressing. If delta is 0, a third word is required to specify a 16-bit address.
2. Flag r is the relative address flag.

3. Flag i is the indirect address flag.

4. Register Ra is the index register.

The addressing modes are similar to the basic storage instructions. The basic set allows indexing by one or two registers (I and Q), while the enhanced set allows indexing by any one of seven registers (1, 2, 3, 4, Q, A, or I). Table 4-8 specifies the addressing modes, the effective address, and the address of the next instruction.

The addressing mode fields determine the effective address for operand A. Register Rb and the instruction mode field (F5) determine the address for operand B. Note that for character addressing, the effective addresses (operand A and register Rb) are combined to ascertain the actual character effective address (refer to the character instructions in table 4-9). Operand B is always the A register for character addressing.

NOTE

For character addressing, selection of absolute (r = 0), no indirect (i = 0), no index register (Ra = 0), and no character register (Rb = 0) results in an EIN instruction.

Any unspecified combinations of F4, F5, and Rb are reserved for future expansion.

The following definitions apply to the description of addressing modes:

- Instruction address – The address of the instruction being executed, also called P.
- Indirect address – A storage address that contains an address rather than an operand. Note that there is no multilevel indirect addressing for enhanced storage reference instructions.
- Base address – The operand address after all indirect addressing but before modification by an index register. The base address is the effective address if no indexing is specified.
- Effective address – The final address of the operand.
- Indexing – If specified, the contents of register Ra are added to the base address to form the effective address. Indexing occurs after addressing is completed.

  The processor uses the 16-bit ones complement adder during indexing operations. Consequently, the index register contents are treated as signed quantities (bit 15 is the sign bit).

- Registers – Registers Ra and Rb are defined as follows.

Register	Value
None	0
1	1
2	2
3	3
4	4
Q	5
A	6
I	7

Enhanced storage reference instructions (table 4-8) have the following types of addressing modes:

- 8-bit absolute – (r = 0, i = 0, and Δ = 0) – The base address equals delta and the sign bit of delta is not extended. The contents of index register Ra, when specified, are added to the base address to form the effective address.

- 8-bit absolute indirect (r = 0, I - 1, and Δ = 0) – The 8-bit value of delta is an indirect address. The sign bit of delta is not extended. The content of this address in low core (addresses 0001_{16} to $00FF_{16}$) is the base address. The contents of index register Ra, when specified, are added to the base address to form the effective address.

- 8-bit relative (r = 1, i = 0, and Δ = 0) – The base address is equal to the instruction address plus one, P + 1, plus the value of delta with sign extended. The contents of index register Ra (when specified) are added to the base address to form the effective address.

  If no indexing takes place, the addresses that can be referenced in the 8-bit relative mode are restricted to the program area. Delta is eight bits long; thus the computer references a location between p - $7E_{16}$ and P + 80_{16} inclusive.

- 8-bit relative indirect (r = 1, i = 1, and Δ = 0) – The address of the second word of the instruction, P + 1, plus the value of delta with sign extended is an indirect address. The content of this address is the base address. The contents of index register Ra, when specified, are added to the base address to form the effective address.

- Absolute constant (r = 0, i = 0), and Δ = 0) – The address of the third word of the instruction, P + 2, is the base address. The contents of the index register Ra, when specified, are added to the base address to form the effective address. Thus when Ra is not specified, the contents of P + 2 is the value of the operand.

  Note that there is no immediate operand condition (that is, indexing is specified and the instruction is a read-operand type) as there is for basic storage reference addressing.

TABLE 4-8. ENHANCED STORAGE REFERENCE INSTRUCTION ADDRESSES

Addressing Mode	Delta	r	i	Ra	Effective Address (EA)	Address of Next Instruction
8-Bit Absolute	$\Delta \neq 0$	0	0	0	Δ	P + 2
		0	0	1	Δ + (1)	P + 2
		0	0	2	Δ + (2)	P + 2
		0	0	3	Δ + (3)	P + 2
		0	0	4	Δ + (4)	P + 2
		0	0	5	Δ + (Q)	P + 2
		0	0	6	Δ + (A)	P + 2
		0	0	7	Δ + (I)	P + 2
8-Bit Absolute Indirect	$\Delta \neq 0$	0	1	0	(Δ)	P + 2
		0	1	1	(Δ) + (1)	P + 2
		0	1	2	(Δ) + (2)	P + 2
		0	1	3	(Δ) + (3)	P + 2
		0	1	4	(Δ) + (4)	P + 2
		0	1	5	(Δ) + (Q)	P + 2
		0	1	6	(Δ) + (A)	P + 2
		0	1	7	(Δ) + (I)	P + 2
8-Bit Relative†	$\Delta \neq 0$	1	0	0	P + 1 + Δ	P + 2
		1	0	1	P + 1 + Δ + (1)	P + 2
		1	0	2	P + 1 + Δ + (2)	P + 2
		1	0	3	P + 1 + Δ + (3)	P + 2
		1	0	4	P + 1 + Δ + (4)	P + 2
		1	0	5	P + 1 + Δ + (Q)	P + 2
		1	0	6	P + 1 + Δ + (A)	P + 2
		1	0	7	P + 1 + Δ + (I)	P + 2
8-Bit Relative Indirect†	$\Delta \neq 0$	1	1	0	(P + 1 + Δ)	P + 2
		1	1	1	(P + 1 + Δ) + (1)	P + 2
		1	1	2	(P + 1 + Δ) + (2)	P + 2
		1	1	3	(P + 1 + Δ) + (3)	P + 2
		1	1	4	(P + 1 + Δ) + (4)	P + 2
		1	1	5	(P + 1 + Δ) + (Q)	P + 2
		1	1	6	(P + 1 + Δ) + (A)	P + 2
		1	1	7	(P + 1 + Δ) + (I)	P + 2

†For these addressing modes, delta is sign extended.

Note: ( ) Denotes contents of expression.

TABLE 4-8. ENHANCED STORAGE REFERENCE INSTRUCTION ADDRESSES (Contd)

Addressing Modes	Delta	r	i	Ra	Effective Address (EA)	Address of Next Instruction
Absolute Constant	Δ = 0	0	0	0	P + 2	P + 3
		0	0	1	P + 2 + (1)	P + 3
		0	0	2	P + 2 + (2)	P + 3
		0	0	3	P + 2 + (3)	P + 3
		0	0	4	P + 2 + (4)	P + 3
		0	0	5	P + 2 + (Q)	P + 3
		0	0	6	P + 2 + (A)	P + 3
		0	0	7	P + 2 + (I)	P + 3
16-Bit Storage	Δ = 0	0	1	0	(P + 2)	P + 3
		0	1	1	(P + 2) + (1)	P + 3
		0	1	2	(P + 2) + (2)	P + 3
		0	1	3	(P + 2) + (3)	P + 3
		0	1	4	(P + 2) + (4)	P + 3
		0	1	5	(P + 2) + (Q)	P + 3
		0	1	6	(P + 2) + (A)	P + 3
		0	1	7	(P + 2) + (I)	P + 3
16-Bit Relative	Δ = 0	1	0	0	P + 2 + (P + 2)	P + 3
		1	0	1	P + 2 + (P + 2) + (1)	P + 3
		1	0	2	P + 2 + (P + 2) + (2)	P + 3
		1	0	3	P + 2 + (P + 2) + (3)	P + 3
		1	0	4	P + 2 + (P + 2) + (4)	P + 3
		1	0	5	P + 2 + (P + 2) + (Q)	P + 3
		1	0	6	P + 2 + (P + 2) + (A)	P + 3
		1	0	7	P + 2 + (P + 2) + (I)	P + 3
16-Bit Relative Indirect	Δ = 0	1	1	0	(P + 2 + (P + 2))	P + 3
		1	1	1	(P + 2 + (P + 2)) + (1)	P + 3
		1	1	2	(P + 2 + (P + 2)) + (2)	P + 3
		1	1	3	(P + 2 + (P + 2)) + (3)	P + 3
		1	1	4	(P + 2 + (P + 2)) + (4)	P + 3
		1	1	5	(P + 2 + (P + 2)) + (Q)	P + 3
		1	1	6	(P + 2 + (P + 2)) + (A)	P + 3
		1	1	7	(P + 2 + (P + 2)) + (I)	P + 3

Note: ( ) denotes contents of expression

TABLE 4-9. ENHANCED STORAGE REFERENCE INSTRUCTIONS

Instruction	Mnemonic	Description
Subroutine/Jump Exit F4 = 5 F5 = 0 Rb = 0	SJE	**Replace the contents of P with the effective address. This instruction can be used as a jump or subroutine exit. For example, if Δ = 1 and Ra has been set up by a previous subroutine jump (see below), control will be returned following that subroutine jump.** **Note that subroutine jumps save the address of the instruction, rather than the next instruction, so the subroutine jump exit may be a two-word instruction (Δ ≠ 0) rather than three.** **For example, the following program makes a subroutine jump at location 1000. Register A will contain 1002 upon entry to the subroutine SUB. Upon completion, SUB will exit to location 1003.** **1000 0446 SJA+ SUB** **1001 5000** **1002 2000** **1003** . . . **2000 SUB** . . . . **2020 0430 SJE- 1, A** **2021 5001** **CAUTION** **Since Rb = 0, a selection of absolute (r = 0), no indirect (i = 0), and no index register (Ra = 0) will result in an EIN instruction.**
Subroutine Jump F4 = 5 F5 = 0 Rb = 1, 2, 3, 4, 5, 6, or 7 r = 1, 2, 3, 4, Q, A, or I	SJr	**Load register r with the address of the last word of this instruction (i.e., P + 1 for Δ ≠ 0; P + 2 for Δ = 0). The contents of P are then replaced with the effective address.**
Add Register F4 = 8 F5 = 0 Rb = 1, 2, 3, 4, 5, 6, or 7 r = 1, 2, 3, 4, Q, A, or I	ARr	**Add (using ones complement arithmetic) the contents of the storage location specified by the effective address to the contents of register r. Operation on overflow is the same as for the ADD instruction. The contents of storage are not altered.**

TABLE 4-9. ENHANCED STORAGE REFERENCE INSTRUCTIONS (Contd)

Instruction	Mnemonic	Description
Subtract Register F4 = 9 F5 = 0 Rb = 1, 2, 3, 4, 5, 6, or 7 r = 1, 2, 3, 4, Q, A, or I	SBr	Subtract (using ones complement arithmetic) the contents of the storage location specified by the effective address from the contents of register r. Operation on overflow is the same as for the ADD instruction. The contents of storage are not altered.
AND Register F4 = A F5 = 0 Rb = 1, 2, 3, 4, 5, 6, or 7 r = 1, 2, 3, 4, Q, A, or I	ANr	Form the logical product (AND), bit-by-bit, of the contents of the storage location specified by the effective address and the contents of register r. The result replaces the contents of register r. The contents of storage are not altered.
AND Memory F4 = A F5 = 1 Rb = 1, 2, 3, 4, 5, 6, or 7 r = 1, 2, 3, 4, Q, A, or I	AMr	Form the logical product (AND), bit-by-bit, of the contents of the storage location specified by the effective address and the contents of register r. The result replaces the contents of the storage location specified by the effective address. The original contents of the storage location (specified by the effective address) replace the contents of the A register. The contents of register r are not altered unless r is the A register. Memory is locked until completion of the instruction. This instruction is useful for communication between processors via memory.
Load Register F4 = C F5 = 0 Rb = 1, 2, 3, 4, 5, 6, or 7 r = 1, 2, 3, 4, Q, A, or I	LRr	Load register r with the contents of the storage location specified by the effective address. The contents of storage are not altered.
Store Register F4 = C F5 = 1 Rb = 1, 2, 3, 4, 5, 6, or 7 r = 1, 2, 3, 4, Q, A, or I	SRr	Store the contents of register r in the storage location specified by the effective address. The contents of register r are not altered.
Load Character to A F4 = C F5 = 2	LCA	Load bits A00 through A08 with a character from the storage location specified by the sum of the effective address and bits 1 to 15 of register Rb. Register Rb bit 0 set to 0 specifies the left character (bits 8 to 15) of the storage location; bit 0 set to 1 specifies the right character (bits 0 to 7). Bits A08 through A15 are not altered.
Store Character from A F4 = C F5 = 3	SCA	Store the contents of bits A00 through A07 into a character of the storage location specified by the sum of the effective address and bits 1 to 15 of register Rb. If bit 0 of register Rb is set to 0, the left character (bits 8 to 15) of the storage location is specified; if bit 0 is set to 1 the right character (bits 0 to 7) is specified. The contents of register A and other storage characters are not altered.

TABLE 4-9. ENHANCED STORAGE REFERENCE INSTRUCTIONS (Contd)

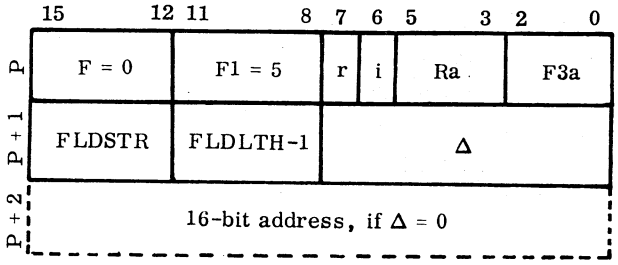
Instruction	Mnemonic	Description
OR Register F4 = D F5 = 0 Rb = 1, 2, 3, 4, 5, 6, or 7 r = 1, 2, 3, 4, Q, A, or I	ORr	Form the logical sum (inclusive OR), bit-by-bit, of the contents of the storage location specified by the effective address and the contents of register r. The result replaces the contents of register r. The contents of storage are not altered.
OR Memory F4 = D F5 = 1 Rb = 1, 2, 3, 4, 5, 6, or 7 r = 1, 2, 3, 4, Q, A, or I	OMr	Form the logical sum (inclusive OR), bit-by-bit, of the contents of the storage location specified by the effective address and the contents of register r. The result replaces the contents of the storage location specified by the effective address. The original contents of the storage location (specified by the effective address) replaces the contents of register A. The contents of register r are not altered unless r is the A register. Memory is locked until completion of the instruction is useful for communication between processors via memory.
Compare Register Equal F4 = E F5 = 0 Rb = 1, 2, 3, 4, 5, 6, or 7 r = 1, 2, 3, 4, Q, A, or I	CrE	Skip one location if the contents of register r and the contents of the storage location specified by the effective address are equal, bit-by-bit. If they are not, execute the next instruction. The contents of register r and storage are not altered.
Compare Character Equal F4 = E F5 = 2	CCE	Skip one location if the contents of bits 0 to 7 of register A and the character of the storage location specified by the sum of the effective address and bits 1 to 15 of register Rb are equal, bit-by-bit. If they are not, execute the next instruction. If bit 0 of register Rb is set to 0, the left character (bits 8 to 15) of the storage location is specified; if bit 0 is set to 1, the right character (bits 0 to 7 is specified. The contents of register A and storage are not altered. **CAUTION** Each compare instruction assumes that a one-word instruction follows it.

- 16-bit storage (r = 0, i = 1, and Δ = 0) – The base address equals the contents of P + 2. The contents of index register Ra, when specified, are added to the base address to form the effective address.
- 16-bit relative (r = 1, i = 0, and Δ = 0) – The base address equals the contents of P + 2 plus P + 2. The contents of index register Ra, when specified, are added to the base address to form the effective address.
- 16-bit relative indirect (r = 1, i = 1, and Δ = 0) – The address of the third word of the instruction, P + 2, plus the contents of the third word of the instruction is an indirect address. The content of this address is the base address. The contents of the index register Ra, when specified, are added to the base address to form the effective address.

The instruction descriptions are given in table 4-9.

FIELD REFERENCE

These instructions have the following format:



Field reference instructions are identified when the F field is 0, the F1 field is equal to 5, and the r, i, Ra, and F3a fields are not all 0. (If these fields are all 0, the instruction is an IIN.)

Field reference instructions contain four parts: operation field (F3a), addressing mode fields (Δ, r, i, and Ra), FLDSTR, and FLDLTH-1 fields. The F3a field determines the operation (for example: load or store). The addressing mode fields are defined exactly as the enhanced storage reference instructions. Refer to table 4-10 for descriptions of these instructions.

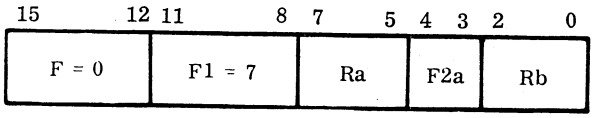
FLDSTR defines the starting bit of the field. For example, FLDSTR = 0 indicates that the field starts at bit 0. FLDLTH-1 defines the length of the field minus one. FLDLTH-1 = 0 indicates that the field is one bit long. If FLDLTH-1 = 0, the field reference instructions become bit reference instructions.

A field starts at the bit specified by FLDSTR and includes the contiguous FLDLTH bits to the right of that bit. No field may cross a word boundry (that is, FLDSTR-FLDLTH-1 must be greater than or equal to 0). If FLDSTR = 0, the field length must be one bit long (FLDLTH-1 =0).

Note that F3a = 0, F3a = 1, and FLDSTR-FLDLTH-1<0 are reserved for future expansion.

ENHANCED INTER-REGISTER

These instructions have the following format:



Enhanced inter-register instructions are identified when the F field is 0, the F1 field is 7, and the F2a, Ra, and Rb fields are not all 0. (If these fields are all 0, the instruction is CPB.)

Enhanced inter-register instructions (similar to the basic inter-register instructions, such as TRA Q) contain three parts: operation field (F2a) and two register fields (Ra and Rb). The F2a field determines the operation (for example, transfer). The Ra and Rb fields specify two operands.

Note that F2a = 1, F2a = 2, F2a = 3, Ra = 0, and Rb = 0 are reserved for future expansion.

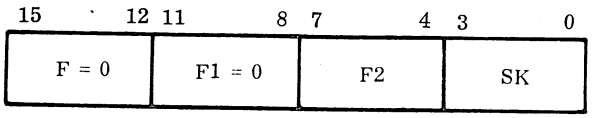
The instruction description is:

Transfer Register — XFr R
F2a = 0
Ra = 1, 2, 3, 4, 5, 6, or 7
r = 1, 2, 3, 4, Q, A, or 1

Transfer the contents of register r to register R. Note that R = 1, 2, 3, 4, Q, A, or I implies that Rb = 1, 2, 3, 4, 5, 6, or 7.

ENHANCED SKIP

The skip instructions have the following format:



Enhanced skip instructions are identified when the F and F1 fields are both 0, and the F2 and SK fields are not both 0. (If these fields are both 0, the instructions is an SLS.)

Enhanced skip instructions (similar to the basic skips, such as SAZ) contain two parts: operation field (F2) and skip count (SK). The F2 field determines the operation (i.e., skip on register 1, 2, 3, or 4 if zero, nonzero, positive, or negative). The skip count specifies how many locations to skip if the skip condition is met.

When the skip condition is met, the skip count plus one is added to the P register to obtain the address of the next instruction (for example, when the skip count is one, go to P + 2). When the skip condition is not met, the address of the next instruction is P + 1 (skip count ignored). The skip count does not have a sign bit.

If F2 = 0 (S4Z), the skip count cannot be 0 because the instruction would be an SLS.

The instruction descriptions are given in table 4-11.

TABLE 4-10. FIELD REFERENCE INSTRUCTIONS

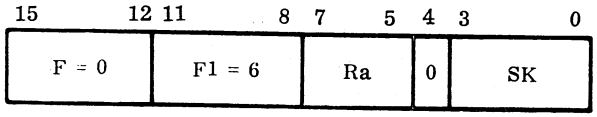
Instruction	Mnemonic	Description
Skip if Field Zero F3a = 2	SFZ	Skip one location if the contents of the specified field of the storage location identified in the effective address are 0 (all bits are 0). If the contents are not 0, execute the next instruction.
Skip if Field Not Zero F3a = 3	SFN	Skip one location if the contents of the specified field of the storage location field identified in the effective address are nonzero (not all bits are 0). If the contents are zero execute the next instruction. **CAUTION** **Each skip field instruction assumes that a one-word instruction follows it.**
Load Field F3a = 4	LFA	Load register A, right justified, with the contents of the specified field of the storage location field identified in the effective address. All other bits of register A are cleared to 0. The contents of storage are not altered.
Store Field F3a = 5	SFA	Store the contents of the field from register A, right justified, into the specified field of the storage location identified in the effective address. All other storage bits are unchanged. Memory is locked until completion of the instruction. The contents of A are not altered.
Clear Field F3a = 6	CLF	Clear the specified field of the storage location specified by the effective address to all 0s. All other storage bits are unchanged. Memory is locked until completion of the instruction.
Set Field F3a = 7	SEF	Set the specified field of the storage location identified in the effective address to all 1s. All other storage bits are unchanged. Memory is locked until completion of the instruction.

TABLE 4-11 ENHANCED SKIP INSTRUCTIONS

Instruction	Mnemonic	Description
Skip if Register Zero F2 = 0, 4, 8, or C r = 4, 1, 2, or 3	SrZ SK	Skip if register r is a positive 0 (all bits are 0).
Skip if Register Nonzero F2 = 1, 5, 9, or D r = 4, 1, 2, or 3	SrN SK	Skip if register r is not a positive 0 (not all bits are 0).
Skip if Register Positive F2 = 2, 6, A, or E r = 4, 1, 2, or 3	SrP SK	Skip if register r is positive (bit 15 is 0).
Skip if Register Negative F2 = 3, 7, B, or F r = 4, 1, 2, or 3	Sr M SK	Skip if register r is negative (bit 15 is a 1).

DECREMENT AND REPEAT

These instructions have the following format:



Decrement and repeat instructions are specified when the F field is 0, the F1 field is 6, bit 4 is 0, and the Ra and SK fields are not both 0. (If these fields are both 0, the instruction is an SPB.)

Decrement and repeat instructions contain two parts: register field (ra) and skip count (SK). The register field specifies which register is to be decremented by one and checked for the skip condition. The skip count specifies how many locations to repeat (go backwards) if the skip condition is met.

When the skip condition is met, the skip count is subtracted from the P register to obtain the address of the next instruction (for example, when the skip count is one, go to P - 1). When the skip condition is not met, the address of the next instruction is P + 1. The skip count does not have a sign bit.

Note that Ra = 0 and bit 4 = 1 are reserved for future expansion.

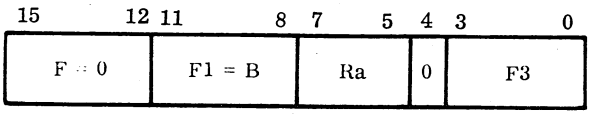
The instruction description is:

Decrement and Repeat if Positive DrP SK
Ra = 1, 2, 3, 4, 5, 6, or 7
r = 1, 2, 3, 4, Q, A, or I

Decrement the contents of register r by one. Operation on overflow is the same as for the ADD instruction. Repeat (go backwards) SK locations if the contents of register r are positive (bit 15 is 0); otherwise, execute the next instruction.

MISCELLANEOUS INSTRUCTIONS

Miscellaneous instructions have the following format:



Miscellaneous instructions are specified when the F field is 0, the F1 field is equal to decimal 11 (hexadecimal B), bit 4 is 0, and the Ra and F3 fields are not both 0. (If these fields are both 0, the instruction is an NOP.) All of the miscellaneous instructions are privileged instructions; that is, if they are executed by an unprotected program, they cause a program protect violation.

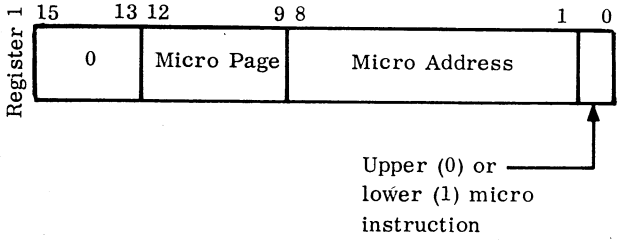
Miscellaneous instructions contain two parts: operation field (F3) and register field (Ra).

If Ra is nonzero, the F3 operation field can select up to 16 miscellaneous instructions with register Ra used to specify an operand. If Ra is 0, the F3 operation field can select up to 15 more miscellaneous instructions without any explicit operand specified.

All the miscellaneous instruction descriptions are given in table 4-12. Those instructions that require more detail are described below. Instructions LRG and SRG are shown in figures 4-1 and 4-2, respectively.

The miscellaneous instructions formats are:

1. Load Micro Memory



Initially, the Q register contains the number of 32-bit micro-memory instructions to be transferred (if Q = 0, no instructions are transferred). Register 1 contains the starting address of micro memory. Register 2 contains the starting address of processor main memory.

The most significant bit (15) of the contents of the starting address is transferred to the most significant bit of the first micro instruction. The least significant bit (0) of the contents of the starting address plus one is transferred to the least significant bit. This instruction is interruptible after storing each 32-bit micro memory instruction and when registers 1, 2, and Q are incremented/decremented to allow the instruction to be restarted after any interruption. When the instruction is completed, these registers contain the following rather than their original values:

Where: i is the initial value before execution.

2. Set/Sample Output or Input

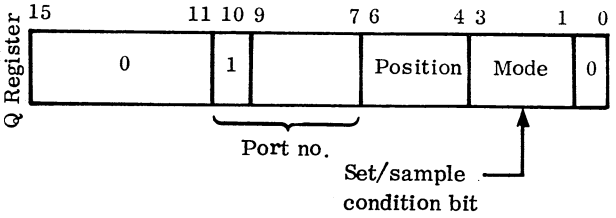


TABLE 4-12. MISCELLANEOUS ENHANCED INSTRUCTIONS

Instruction	Mnemonic	Description
Load Micro Memory F3 = 1 Ra = 0	LMM	Load a 32-bit micro-memory instruction into read/write micro memory from 16-bit processor main memory. (For read-only micro memory or no micro memory, no operation is executed.)
Load Registers F3 = 2 Ra = 0	LRG	Registers 1, 2, 3, 4, Q, A, I, M, and the overflow indicator are loaded with the contents of nine storage locations, beginning at a storage location specified by the contents of the contents of the next location, P + 1. The contents of the nine storage locations will not be altered and the next instruction will be executed at location P + 2 (i.e., the LRG instruction is a two-word instruction). Refer to figure 4-1.
Store Registers F3 = 3 Ra = 0	SRG	Registers 1, 2, 3, 4, Q, A, I, M, and the overflow indicator are stored into nine storage locations specified by the contents of the next location, P + 1, incremented by a decimal 10. The contents of the registers will not be altered and the next instruction will be executed at location P + 2 (i.e., the SRG instruction is a two-word instruction). Refer to figure 4-2.
Set/Sample Output or Input F3 = 4 Ra = 0	SIO	Set one word from register A for output to an external device. The word in register Q selects the receiving device. For input, one word from an external device is sampled (input) to register A. The word in register Q selects the sending device.
Sample Position/Status F3 = 5 Ra = 0	SPS	Sample (input) to the A register the position and status of a M05 device, which has caused a processor macro interrupt. The word in the Q register selects the device. The instruction also provides for clearing the M05-generated processor macro interrupt.
Define Micro Interrupt F3 = 6 Ra = 0	DMI	Define the use of one of the 12 available micro interrupts. (The use of micro interrupts 12 through 15 is restricted for internal use.) This instruction allows a micro interrupt to be enabled/disabled and defined for auto-data transfer (ADT) or special usage.
Clear Breakpoint Interrupt F3 = 7 Ra = 0	CBP	Clear the processor macro breakpoint interrupt. This interrupt occurs when the following conditions are true: macro breakpoint is externally selected, macro breakpoint interrupt option is externally selected, the MP recognizes a breakpoint condition and generates a macro breakpoint interrupt because of b.
Generate Character Parity Even F3 = 8 Ra = 0	GPE	Set or clear bit 7 of the A register so that bits 0 to 7 have an even parity. The other bits in the A register are not altered.
Generate Character Parity Odd F3 = 9 Ra = 0	GPO	Set or clear bit 7 of the A register so that bits 0 to 7 have an odd parity. The other bits in the A register are not altered.

TABLE 4-12. MISCELLANEOUS ENHANCED INSTRUCTIONS (Contd)

Instruction	Mnemonic	Description
Scale Accumulator F3 = A Ra = 0	ASC	Shift the A register left (end-around) until bits 14 and 15 of the A register are different. Upon completion of the instruction, register 1 contains the number of spaces that the A register was shifted. (This number may range from 0 to 14.) If the A register is ±0 (000 or FFFF), no shift has been performed and register 1 contains -0 ($FFFF_{16}$).
Absolute Page Mode F3 = B Ra = 0	APM	Absolute page mode is specified. Only the first 65,536 words of memory can be addressed.
Page Mode Zero F3 = C Ra = 0	PM0	Page mode 0 is specified. Segments of 2,048 words, totaling 65,536 words, can be addressed via the 32-word page mode 0 register file.
Page Mode One F3 = D Ra = 0	PM1	Page mode 1 is specified. Segments of 2,048 words, totaling 65,536 words, can be addressed via the 32-word page mode 1 register file.
Load Upper Unprotected Bounds F3 = 0 Ra = 1, 2, 3, 4, 5, 6, or 7 R = 1, 2, 3, 4, Q, A, or I	LUB R	Load the upper unprotected bounds register from the contents of register R.
Load Lower Unprotected Bounds F3 = 1 Ra = 1, 2, 3, 4, 5, 6, or 7 R = 1, 2, 3, 4, Q, A, or I	LLB R	Load the lower unprotected bounds register from the contents of register R.
Execute Micro Sequence F3 = 2 Ra = 1, 2, 3, 4, 5, 6, or 7 R = 1, 2, 3, 4, Q, A, or I	EMS R	Transfer machine control to the upper micro instruction of the page/micro-memory address in bits 0 thorugh 15 of register R. A section of micro memory is assumed to have been previously loaded.
Write Page Register F3 = 3 Ra = 1, 2, 3, 4, 5, 6, or 7 R = 1, 2, 3, 4, Q, A, or I	WPR R	Write the contents of register R, bits 0 through 8, into the page register specified by bits 10 through 15 of register R. Bit 10 is zero or one for a page mode 0 or 1 register, respectively. Bits 11 through 15 specify one of the 32-page registers within the page mode. Bit 9 is unused and should be zero.
Read Page Register F3 = 4 Ra = 1, 2, 3, 4, 5, 6, or 7 R = 1, 2, 3, 4, Q, A, or I	RPR R	Read the contents of the page register, specified by bits bits 10 through 15 of register R into the A register. Bit 10 is zero or one for a page mode 0 or 1 register, respectively. Bits 11 through 15 specify one of the 32-page registers within the page mode. Bits 0 thorugh 9 are unused and should be zero.
Read ECC Status F3 = 5 Ra = 1, 2, 3, 4, 5, 6, or 7 R = 1, 2, 3, 4, Q, A, or I	ECC R	Read the error checking and correction status of the memory word, specified by the address in register R, into the A register.

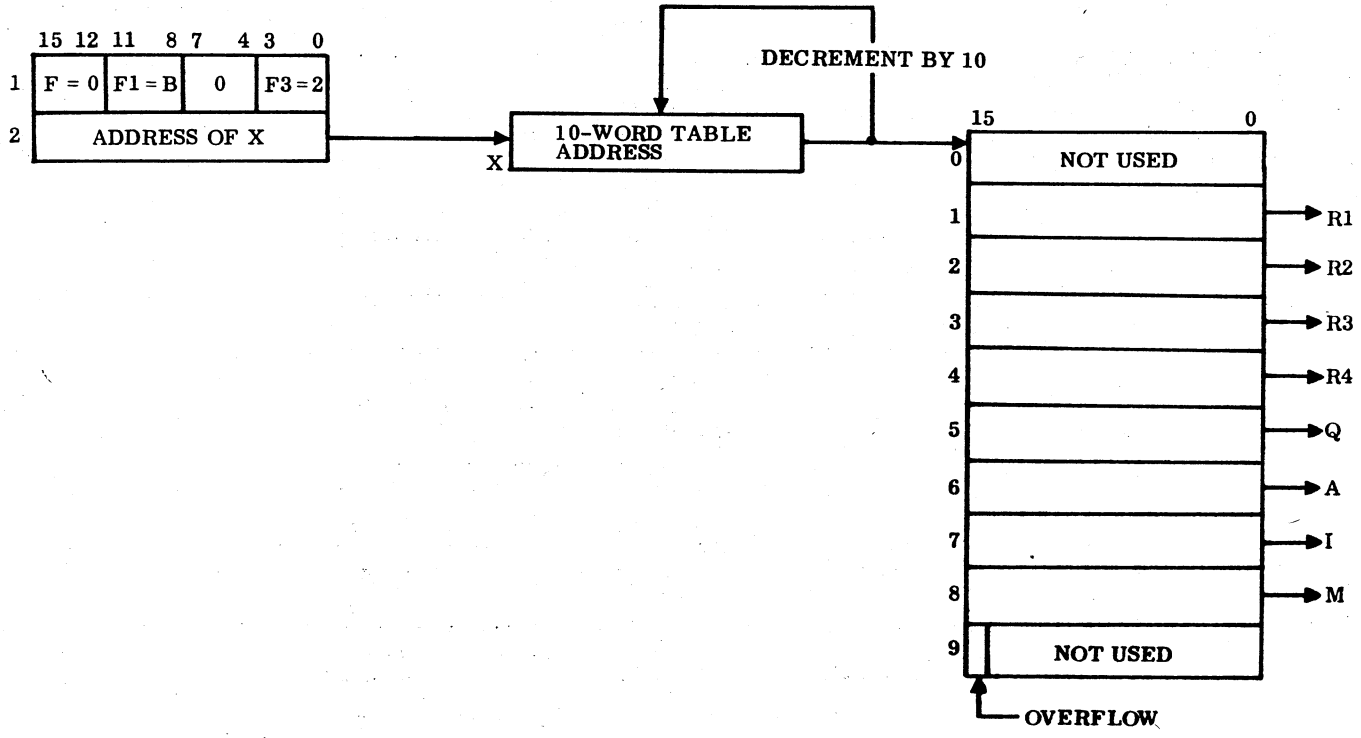


Figure 4-1. LRG Instruction

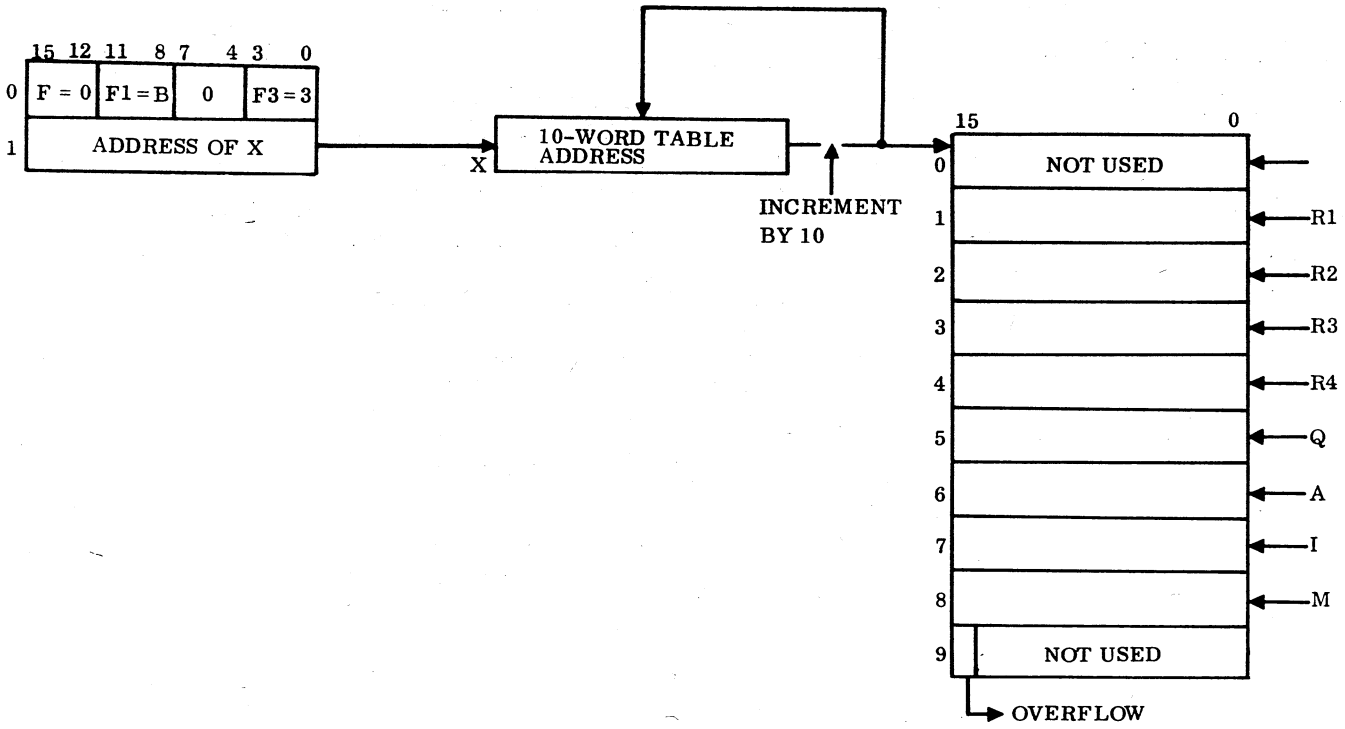
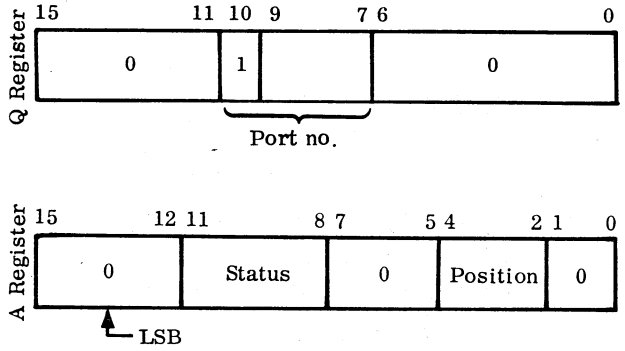
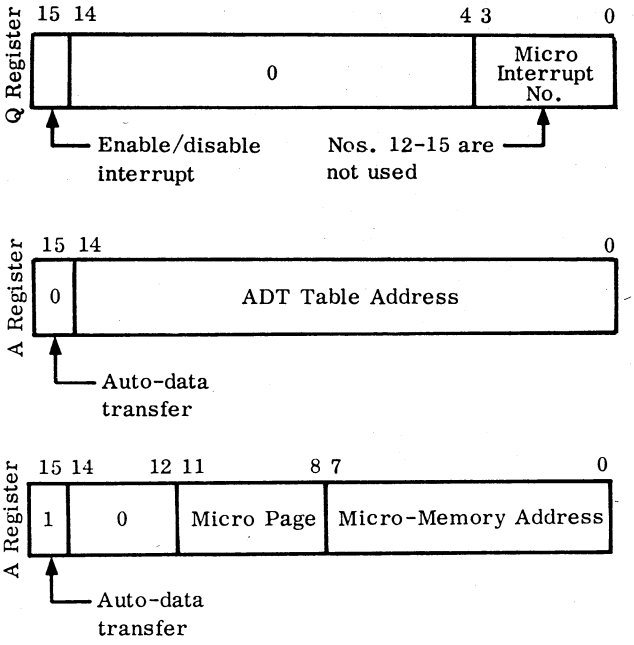


Figure 4-2. SRG Instruction

3. Sample Positions Status



4. Define Micro Interrupt

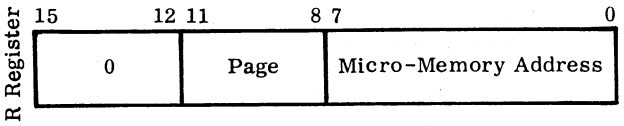


When bit 15 of the A register is set to a 1, a jump is made to the upper micro instruction of the page/micro memory in bits 0 to 14. A section of micro memory is assumed to have been previously loaded, and it must process the micro interrupt properly and return control to the current macro instruction address (P) by jumping to the lower micro instruction of micro-memory address $3E_{16}$ in micro page 0. Registers P, A, Q, and all of file 2 should not be altered, and return must be within 12.5 microseconds.

CAUTION

The processor micro function, SUB-, must not be used. Extreme caution should be exercised in using this option, since it provides an escape from the 1700 emulation being performed.

5. Execute Micro Sequence

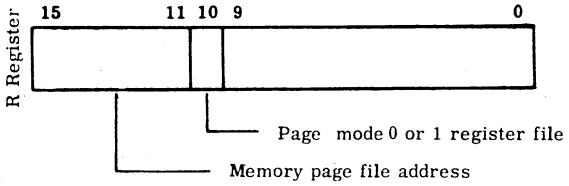


An execute micro sequence to nonexistant micro memory may cause an indeterminate result. Control should be returned to the next macro-instruction address (P + 1) by jumping to the lower micro instruction of micro-memory address 3E in micro page 0. Registers P, A, Q, and all of file 2 should not be altered, and return must be within 12.5 microseconds (or the micro sequence must be interruptible).

CAUTION

Extreme caution should be exercised in using this option, since it provides an escape from the 1700 emulation being performed.

6. Write Page Register

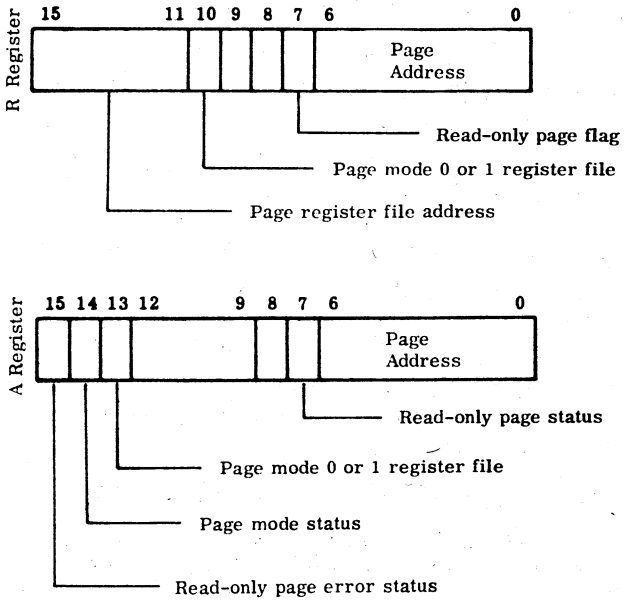


This command loads a page address into a page register file (memory page file) in main memory.

When bit 10 of the R register is zero, one of the 32 locations that corresponds to the page mode 0 register file specified by bits 11 through 15 is loaded with the information contained in bits 0 through 8 of the R register. If bit 10 is a one, one of the 32 locations that corresponds to the page mode 1 register file is loaded. Bits 0 through 8 represent the page address, which forms the seven most significant bits of the 18-bit main memory address (256K-word addressing). Bit 7, if a one, establishes the page as a read-only page (see section 6, Program Protect). To write into any page location on a page mode main memory write reference, this bit must be set to 0. Bit 9 is unused and should be zero.

A write page register instruction clears a read-only page interrupt.

7. Read Page Register

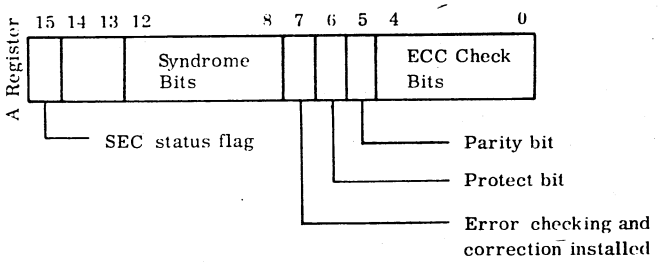


The page register is referenced as described for a write page register instruction.

Bits 0 through 8 of the A register are loaded with the contents of the referenced page register. Bits 0 through 6 contain the 7-bit stored page address; bit 7 contains the read-only page bit for that page. Bits 8 through 12 are unused and are zero.

Bits 13 through 15 of the A register contain status information from main memory. Bit 13 indicates the page mode register set selected. Bit 14 shows that main memory is in absolute mode if zero, page mode if one. Bit 15 indicates a read-only page error. A read page register instruction clears this error bit.

8. Read ECC Status



This instruction loads main memory status information into the A register. The address in register R may be either absolute or page mode format, appropriate for the main memory mode previously selected.

In the A register, bits 0 through 4 are the five ECC bits for the addressed word. Bit 5 is the parity bit, and bit 6 is the program protect bit. Bit 7 is a one if the ECC option is installed.

Bits 8 through 12 are the ECC syndrome bits, which should all be zero if no memory errors exist. Bit 15 is the single error correction (SEC) status flag, which is set if a single bit main memory error has occurred on a read or normal write operation. The single error correction status flag is set on single bit errors only if ECC is installed (the error is automatically corrected). If ECC is not installed, a single bit error causes a parity error.

A Read ECC Status instruction clears the single error correction status flag in main memory.

AUTO-DATA TRANSFER

Auto-data transfer provides for pseudo direct memory transfers of data blocks to or from a device. At the macro level, the transfer appears as a direct memory access (DMA) transfer. At the micro level, the 1700 emulator processes each data interrupt and inputs or outputs the next data in a singular fashion. Thus, auto-data transfer takes less time than input/output via the INP, OUT, or SIO instructions, but more time than a true DMA transfer.

To accomplish an auto-data transfer for a particular device, perform the following:

- The device and its controller must be capable of operating in the auto-data transfer mode.
- The macro programmer must initialize the auto-data transfer that is defined by the DMI instruction.
- The macro programmer must execute a DMI instruction. This command specifies where the block of data is, how long it is, the direction (input/output), and the device's address.
- The auto-data transfer operation is then initiated by an INP, OUT, or SIO instruction as specified by the particular device.

While the auto-data transfer operation is in progress, the emulator is executing instructions. After each instruction is executed, interrupts are checked. When the particular auto-data transfer micro interrupt becomes the highest active interrupt, the next data is input or output. After the interruption, the next instruction is executed, except when another interrupt is active.

When the auto-data transfer operation is completed (or if there is an error), a macro interrupt is generated. The macro programmer may then disable the auto-data transfer micro interrupt or initiate another auto-data transfer operation to or from the device. For MOS devices, an SPS instruction must be performed to clear the macro interrupt.

The following are the four types of auto-data transfer tables specified by DMI instructions.

1. Auto-Data Transfer Table for a Single A/Q Device:

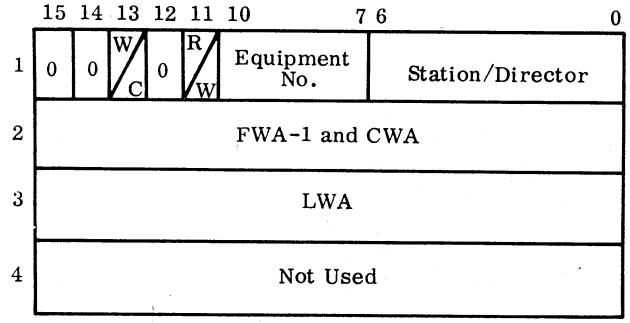
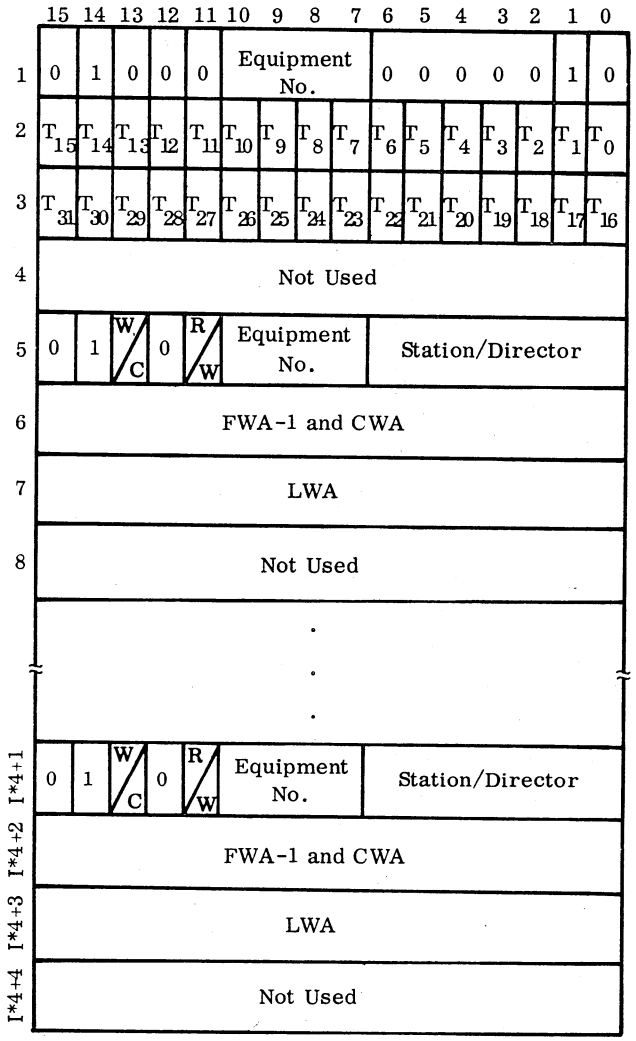


Table 4-13 gives a detailed description of these four words.

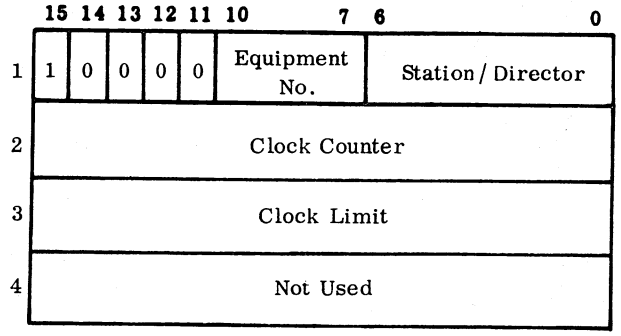
2. Auto-Data Transfer Table for Multiple A/Q Devices:



This type of auto-data transfer table consists of I*4+4 words, where 1 is the number of multiple A/Q devices (up to 32) on one micro interrupt.

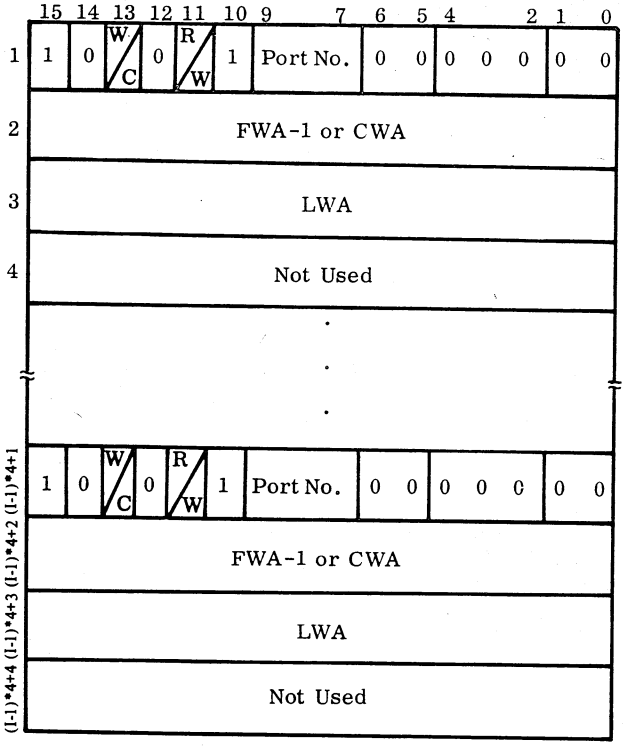
Table 4-14 provides detailed descriptions of these words.

3. Auto-Data Transfer Table for the Clock:



Detailed descriptions of this type are given in table 4-15.

4. Auto-Data Transfer Table for Single or Multiple M05 Devices



The auto-data transfer table for this type consists of (I-1)*4+4 words, where I is the number of M05 devices (up to 8) on one micro interrupt. Detailed descriptions of this type are given in table 4-16.

TABLE 4-13. ADT TABLE FOR A SINGLE A/Q DEVICE

Word	Bits	Description
1	15 14 12	Must be set to 0.
	13	0 Word operation; data is transferred one word at a time. Normally, a total of (CWA - FWA + 1) words will be transferred. 1 Character operation; data is transferred one character (eight bits) at a time. On input, the first character will be stored in the most significant half (bits 15 to 8) of the current words address; the second character in the least significant half (bits 7 to 0). Subsequent pairs of characters will be output from the most significant half of the current word address; the second character from the least significant half. Normally a total of 2 × (CWA - FWA + 1) characters will be transferred.
	11	0 A read ADT operation 1 A write ADT operation
	10 through 7	The equipment number of the device. This number can not conflict with any MO5 I/O port numbers.
	6 through 0	The station/director bits of the device to execute the ADT operation. These bits should specify a data (not a status/function) transfer.
2		Initially set to the first word address less one (FWA - 1) of the data block to be transferred. This word is used as the current word address (CWA) as the ADT operation is in progress and points to the last word read or stored. Each time a word (or two characters) is transferred, CWA is incremented. Specifically, CWA can be used to ascertain whether all the data was transferred after the ADT operation was completed (if CWA = LWA, all the data has been transferred).
3		The last word address (LWA) of the data block to be transferred
4		Reserved for future use; must be set to 0.

TABLE 4-14. ADT TABLE FOR MULTIPLE A/Q DEVICES

Word	Bits	Description
1	15	Must be 0
	14	Must be 1
	13 through 11	Must be 0
	10 through 7	The equipment number of the device. This number can not conflict with any M05 I/O port numbers.

TABLE 4-14. ADT TABLE FOR MULTIPLE A/Q DEVICES (Contd)

Word	Bits	Description
	6 through 2	The maximum station (or channel) number; equivalent to the number of multiple A/Q devices less one on a wire interrupt. Station numbers must be contiguous. Certain peripheral devices have specific parameters for these bits; refer to the peripheral controller reference manual.
	1	Must be 1
	0	Must be 0
2 3		Contain termination bits for the 32 devices. Initially, they must be all 0. When a macro interrupt occurs, one or more of these bits will be set to 1 to indicate that one or more ADT operations have terminated. Thus $T_7 = 1$ indicates that the seventh device has terminated its ADT operation. After receipt, the bit should be cleared via an instruction that locks memory (e.g., a CLF instruction).
4		Reserved for future use; must be 0.
5 6 7 8 †		Defined the same as a single A/Q device, except for bit 14 of the first word (I*4+1), which must be 1. Refer to table 4-13.

† Words I*4+1, I*4+2, I*4+3, and I*4+4, where $2 \leq I \leq 32$

TABLE 4-15. ADT TABLE FOR THE CLOCK

Word	Bits	Description
1	15	Must be 1
	14 through 11	Must be 0
	10 through 7	The equipment of the clock; must be set to 1.
	6 through 0	The station/director bits of the clock, which is always equal to 70_{16}. (Thus, word 1 should equal $80F0_{16}$.)
2		Initially set to 0; whenever the clock has been enabled, the clock counter will be incremented every 3 1/3 milliseconds.

TABLE 4-15. ADT TABLE FOR THE CLOCK (Contd)

Word	Bits	Description
3		The clock limit, which is interpreted as a multiple of 3 1/3 milliseconds. When the clock counter equals the clock limit and the macro-clock interrupt is enabled, the macro-clock interrupt will occur. Thus, if the clock limit is five, the clock interrupt is 16 2/3 milliseconds, or 60 times a second. To continue the process, the clock counter should be reset to 0, or the limit counter should be incremented by its original value (e.g., 5). In the latter method, the clock counter can function as an elapsed time counter. Note that if the macro-clock interrupt is not answered the clock limit will still continue to be incremented.
4		Reserved for future use; must be 0.

TABLE 4-16. ADT TABLE FOR SINGLE OR MULTIPLE M05 DEVICES

Word	Bits	Description
1	15	Must be 1
	14	Must be 0
	13	Defined the same as a single A/Q device.
	12	Must be 0
	11	0 A read ADT operation 1 A write ADT operation
	10 through 7	The part number of the device. (Bit 10 is always set to 1.) Part numbers are analogous to the A/Q I/O equipment numbers and thus cannot conflict with them.
	6, 5	Must be 0
	4 through 2	The maximum position number; equivalent to the number of multiple M05 devices, less one, on a wire interrupt. Position numbers must be contiguous (i.e., 0 to I-1).

TABLE 4-16. ADT TABLE FOR SINGLE OR MULTIPLE M05 DEVICES (Contd)

Word	Bits	Description
2†		Initially set to the first word address (FWA-1) of the data block to be transferred; this word is used as the current word address (CWA) as the ADT operation is in progress and points to the last data word read or stored. Each time a word (or two characters) is transferred, CWA is incremented. Specifically, CWA can be used to ascertain whether all the data was transferred after the ADT operation was completed (i.e., if CWA = LWA, all data has been transferred).
3†		The last word address (LWA) of the data block to be transferred
4†		Reserved for future use; must be 0.

† Words (I-1)*4+1, (I-1)*4+2, (I-1)*4+3, and (I-1)*4+4, where $2 \leq I \leq 8$, are defined in the same manner as words 1, 2, 3, and 4, respectively.

This system enables the program to establish a priority so that a high priority interrupt can interrupt the machine while it is processing a low priority interrupt. The return path to the interrupted program is clearly established and saved.

INTERRUPT TRAP LOCATIONS

Trap locations are established for each interrupt line. They are in the range of address 0100 through 013C. These addresses are reserved for interrupts unless that particular interrupt is not being used. The assignment for each interrupt state or line is shown in table 5-1.

MASK REGISTER

The mask register is the enable for each interrupt state or line. Bit 0 of the mask register corresponds to interrupt line 0, bit 1 to line 1, etc. To enable an interrupt line, its corresponding bit in the mask register must be set. The mask register is set by the inter-register instruction.

PRIORITY

The computer program controls the interrupt priority by establishing a mask for each interrupt state, which enables all higher priority interrupts and disables all lower priority

TABLE 5-1. INTERRUPT STATE DEFINITIONS

Interrupt State	Value of Δ to Exit State	Location of Return Address	Location of First Instruction after Interrupt Occurs
00	00	0100	0101
01	04	0104	0105
02	08	0108	0109
03	0C	010C	010D
04	10	0110	0111
05	14	0114	0115
06	18	0118	0119
07	1C	011C	011D
08	20	0120	0121
09	24	0124	0125
10	28	0128	0129
11	2C	012C	012D
12	30	0130	0131
13	34	0134	0135
14	38	0138	0139
15	3C	013C	013D

interrupts. When an interrupt state is entered, the mask for that state is placed in the mask register. Therefore, there may be up to 16 levels of priority. It is possible to change priority during execution of a program.

INTERNAL INTERRUPTS

Interrupts are also generated by certain conditions arising within the computer. These are called internal interrupts. If such a condition occurs, it generates interrupt 00 (interrupt mask bit 00). Normally, internal interrupts are assigned the highest priority. The internal interrupts are:

- Storage parity error
- Program protect fault
- Power Failure

OPERATION

The computer can distinguish between up to 16 (1 internal, 15 external) macro interrupts. Each of these interrupts has its respective address to which control is transferred when the interrupt is recognized.

When the computer is processing a particular interrupt, it is defined as being in that interrupt state (state 00 through 15). Thus, the interrupts and their respective bits in the interrupt mask register are numbered 00 through 15. An interrupt in bit 7 puts the computer in interrupt state 7, etc.

Before the computer can recognize any interrupt, the mask bit for that interrupt must be set and the interrupt system must be activated. The mask register may be set by an inter-register command and the interrupt system can be activated by an enable interrupt command.

When an interrupt is recognized, the computer automatically stores the return address in the storage location reserved for that interrupt state. If 32K mulitlevel indirect mode has been selected, bit 15 of the storage location is set or cleared to record the current state of the overflow indicator. If 65K multilevel indirect mode has been selected, all 16 bits are required to save the return address. Thus, the program must check for an overflow condition with an SOV or SNO instruction and record this condition for restoration of the overflow indicator. In both 32K and 65K modes, the interrupt system is de-activated and control is transferred when the interrupt occurs. In 32K mode, the overflow is cleared; while in 65K mode, the SOV or SNO instruction must first be executed. The program then stores all registers, including the mask register, in addresses reserved for this interrupt state and loads the mask register with the mask to be used in this state. The 1s in the mask indicate the interrupts that have a higher priority than the interrupt being processed. The mask should not have a 1 in the position of the interrupt being processed; this loses the return link. The program then activates the interrupt system and processes the interrupt.

The computer exits from an interrupt state when the program inhibits the interrupt and restores the registers (including the mask register). After loading the register, the program executes the exit interrupt command with delta equal to the lower eight bits of the base address of the interrupt state. This command reads the storage location where the return address is stored. The overflow indicator is set or cleared as specified by bit 16. The interrupt system is activated and control is transferred to the return address.

Example:

The following listing and sample program steps apply if there were five different possible interrupts and three levels of priority:

Interrupt 01		High priority
02		Mid-priority
05		
03		Low priority
04		

Bit	5 4 3 2 1 0	
Mask 1	1 1 1 1 1 1	Mask used for main program
Mask 2	1 0 0 1 1 1	Mask used for state 03, 04
Mask 3	0 0 0 0 1 1	Mask used for state 02, 05
Mask 4	0 0 0 0 0 1	Mask used for state 01

Main Program

Set mask register to mask 1
Enable interrupt
.
.
.

State 01 Program

Store registers
Set mask to mask 4
Enable interrupt
.
.
.
Inhibit interrupt
Exit interrupt 01

State 02 Program

Store registers
Set mask to mask 3
Enable interrupt
.
.
.
Inhibit interrupt
Replace registers
Exit interrupt 02

State 03 Program

Store registers
Set mask to mask 2
Enable interrupt
.
.
.
Inhibit interrupt
Replace registers
Exit interrupt 03

State 04 Program

Store registers
Set mask to mask 2
Enable interrupt
.
.
.
Inhibit interrupt
Replace registers
Exit interrupt 04

State 05 Program

Store registers
Set mask to mask 3
Enable interrupt
.
.
.
Inhibit interrupt
Replace registers
Exit interrupt 05

The processor has two program protect systems to protect a program in the processor from any other unprotected program also in the processor. The first and highest priority system is available only in page mode operation. Entire 2K word pages may be established as read-only pages and may not be changed until the read-only page protection is removed. The second sytem may be implemented on either absolute or page mode and is built around a program protect bit contained in each word of storage. If the bit is set, the word is an operand or an instruction of the protected program. Main memory bounds registers are also provided that are used to override the protect system. In effect, they define a section of memory that behaves as if the program protect bits are off.

READ-ONLY PAGE PROTECTION

Once a page has been designated a read-only page, no write attempt by the CPU in page mode can alter the contents of any words within that page. Any such attempt by either a protected or unprotected instruction is ignored by memory, and the read-only page error status flag is set in memory. The condition of the read-only status flag can be determined by executing an RPR instruction (0Bx4); the flag condition is then available to the CPU as bit 7 of the A register.

The establishment of a read-only page is made by setting bit 7 in the R register before a WPR instruction. The read-only page status is cleared in the same manner by clearing bit 7 in the R register before a WPR instruction.

Words contained within a read-only page may be altered under the four following conditions:

- A write instruction by the CPU operating in absolute mode (first 65K words only); the read-only page protection is not sensed in absolute mode.
- A write instruction by the CPU in page mode via a different page register containing a duplicate page address without the read-only page bit set (the same page address in two or more page registers)
- A write instruction from a DMA peripheral; The read-only page protection is not sensed on DMA operations.
- In a dual CPU configuration, a write instruction from the second CPU; the read-only page protection initiated by the local CPU is not sensed.

To completely protect against external alterations to a read-only page, the program protect bit system should also be employed. Since the program protect bit is stored with each word, its condition is sensed regardless of the source of the instruction.

PROGRAM PROTECT BIT PROTECTION

All operand and instruction locations of a protected program must have the program protect bit set. None of the instructions or write operands of the unprotected program can have the program protect bit set.

Program protect is enabled by setting bit 8 in the function control register. If this bit is not set, none of the following violations are recognized.

PROGRAM PROTECT VIOLATIONS

Whenever a violation of the program protect system is detected, other than a DMA or remote CPU violation, the program protect fault flip-flop is set and an internal interrupt is generated. A violation indicates that the unprotected program has attempted an operation that could harm the protected program.

The following are the program protect violations:

- An unprotected instruction attempts to write in a protected storage location. The contents of the storage location are not changed.
- An attempt is made to write into a protected storage location via a protected DMA device when an unprotected instruction was the ultimate source of the attempt. The contents of the storage location are not changed.
- An attempt is made to execute a protected instruction following execution of an unprotected instruction. The protected instruction is executed as an unprotected selected stop instruction. However, it is not a violation if an interrupt caused this sequence of instructions.
- An attempt is made to execute the following instructions when they are not protected: any inter-register instructions with bit 0 equal to 1 (attempt to change the contents of the mask register), EIN, IIN, EXI, SPB, CPB, or any miscellaneous instructions (0Bxx). Those instructions become an unprotected selective stop instruction under these circumstances.

SET/CLEAR PROGRAM PROTECT BIT

The program protect instructions (SPB or CPB) are the only way in which the program protect bit may be set or cleared in each word of storage by the processor. The condition of the protect bit in each word remains unchanged through subsequent write instructions until a set/clear protect bit instruction is again employed.

BOUNDS REGISTER OPERATION

The main memory bounds registers are used to override the protect system. In effect, they define a section of memory that behaves as if the program protect bits are off. When a processor logical address is greater than the lower bounds address and less than the upper bounds address, the referenced location is an unprotected memory location regardless of the state of the protect bit. Note that the bounds register address locations themselves are not in the unprotected area.

In page mode, the bounds addresses apply to the logical address (that is, the 16-bit address consisting of a 5-bit page address and 11-bit word address). The bounds address comparison is made before the conversion through the page register file to a physical memory address, and therefore the unprotected area may be scattered throughout the physical memory.

In absolute mode, the bounds are applied to the absolute memory address and are therefore restricted to the first 65K words of memory. Since the affected memory locations change when switching between addressing modes with APM, PM0, or PM1 instructions, the bounds addresses should be reloaded.

The bounds registers are always in operation and are loaded using LLB and LUB instructions. To remove the affect of the bounds registers, load the upper bounds register with address 0.

The bounds registers have no effect on DMA or remote processor references to the main memory.

STORAGE PARITY ERRORS AS RELATED TO PROGRAM PROTECTION

If an unprotected instruction is attempting to write into storage (the program protect system is enabled) and a storage parity error is present or occurs, the word in storage is not altered and a storage parity error interrupt is generated.

If a protected instruction is attempting to write into storage and a storage parity error occurs, the word is written into storage and a storage parity error interrupt is enabled.

If the computer attempts to execute an SPB or CPB instruction (the program protect system is enabled) and a storage parity error occurs, these become NOP instructions and a storage parity error interrupt is enabled.

On units with error checking and correction, a storage parity error is generated only on a 2-bit memory error. Single bit errors, including an error in the protect bit, are corrected and the operation continues as if no error had occurred.

PROGRAMMING REQUIREMENTS

The following program requirements must be met:

- The program package that handles all interrupts for the unprotected program must be part of the protected program.
- The protected program should be a completely checked out program.

PERIPHERAL EQUIPMENT PROTECTION

All peripheral equipment essential to the operation of the protected program must have a switch to designate if the device is protected. If the switch is set, the peripheral device responds with a reject to all unprotected commands (except status request) addressed to it. All protected commands have a normal response. If the switch is not set, the peripheral device responds in the normal manner to protected and unprotected commands.

The standard assignments for system identification devices are listed in table 7-1. Descriptions of the panel/program device and clock follow.

PANEL/PROGRAM DEVICE

When referencing the panel/program devices, the Q register should contain either 0090_{16} or 0091_{16} according to the following table.

	Computer Instruction	
Q Register	Output from A	Input to A
0090	Write	Read
0091	Director function (1)	Director status (2)

DIRECTOR FUNCTION (1)

Bit (A Register)	Function	Operation
00	Clear controller	Clear all interrupt requests. Clear busy, interrupt, data, alarm, and manual interrupt conditions. Select read mode. Connect printer. Any interrupt request bit takes precedence over this function. Clear controller is also used in conjunction with bits 11, 12, 14, and 15.
01	Clear interrupt	Clear all interrupt requests and the manual interrupt. Any interrupt requests bit takes precedence over this function.
02	Data interrupt request	Send an interrupt signal whenever a data status is active.
03	End-of-operation interrupt request	Send an interrupt signal when the controller is not busy. In the end-of-operation state, the controller accepts a mode change.
04	Alarm interrupt request	Send an interrupt signal when the lost data status is active.
05	Not used	
06	Auto-data transfer mode	Auto-data transfer operation
07	Not used	
08	Select write mode	An output operation; does not clear the alarm status
09	Select read mode	An input operation
10	Connect printer	Select a mode of operation in which the printer (with the paper tape punch, when used) and the tape reader (when used) are both connected to the controller. Data read from the paper tape in this mode is also printed (and punched).
11	Not used	
12	Not used	
13	Disconnect printer	Select a mode of operation in which the printer (and paper tape punch when used) is disconnected from the controller. Data read from paper tape is not printed (or punched). This mode allows non-ASCII codes and binary information to be transmitted to the computer.
14	Not used	
15	Not used	

All nonconflicting functions may be performed simultaneously. Select write mode and select read mode are rejected when the controller is busy. Other functions are always performed. When several functions are issued simultaneously and some of them can be performed, the output from the A instruction exists normally (reply), but those functions that should be rejected are not performed. When none of the functions can be performed, the output from the A instruction is rejected.

TABLE 7-1. STANDARD EQUIPMENT/INTERRUPT ASSIGNMENTS FOR CYBER 18-10/20/30 TIMESHARE

Peripheral	Equipment† Code	Macro Interrupt	Micro Interrupt
Teletypewriter/console display	1	1	1
Paper tape reader	2	2	2
Paper tape punch	2	2	2
Card punch	2	2	2
None	3	3	3
Line printer	4	4	4
None	5	5	5
None	6	6	6
Tape cassette	7	7	7
Clock	1	8	8
Magnetic tape transport (NRZI only)††	9	9	0,9
Eight-channel communication line adapter	10	10	10
Dual-channel communication line adapter	10	10	10
Card reader	11	11	11
Magnetic tape transport (NRZI, phase encoded)	12	12	N/A
IOM	13	13	N/A
Storage module drive	14	14	N/A
Cartridge disk drive	14	14	N/A
Flexible disk drive	15	15	N/A
Protect, parity, and power failure (internal)	N/A	0	N/A
Macro stop and panel (internal)	N/A	N/A	12 through 15

†Equipment codes 0 and 8 are currently unassigned and reserved for future use.

††The magnetic tape transport (NRZI only) micro interrupt is wired to both micro interrupt 0 and 9. The software has the responsibility to select the desired one.

DIRECTOR STATUS (2)

Bit (A Register)	Status	Description
00	Ready	Unit is ready.
01	Busy	Read mode – The controller is in the process of receiving a character from the teletypewriter/console display, or the holding register contains data for transfer to the computer. The busy status drops upon completion of the data transfer. Write mode – The data register contains data and is in the process of transferring it to the teletypewriter/console display. The busy status drops when the transfer is completed.
02	Interrupt	An interrupt condition exists in the controller.
03	Data	Read mode – The holding register contains data for transfer to the computer. The data status drops when the transfer is completed. Write mode – The controller is ready to accept another character from the computer.
04		Always the inverse of busy (bit 01)
05	Alarm	Parity error or lost data or field error (no stop bit when expected) occurred.
06	Lost data	The holding register contained data for transfer to the computer, and the teletypewriter/console display began to send a new sequence.
07	Parity error	A parity error occurred.
08	Release	Release reserve interrupt; this interrupt is generated when the console display or teletypewriter has been reserved for the panel interface and is returned.
09	Read mode	The controller is conditioned for input operation.
10	Reserved	Indicates if the teletypewriter or console display is currently assigned to the panel interface and is unavailable to the teletypewriter controller.
11	Manual interrupt	A manual interrupt has occurred.
12	Not used	Always 0
13	Not used	Always 0
14	Not used	Always 0
15	Not used	Always 0

REAL-TIME CLOCK

The real-time clock is an integral part of the I/O module and is designed to appear as a 1700 peripheral to the macro-level software. Two functions are available to the macro-level program: enable/disable limit interrupt and enable/disable clock. Also available to the macro-level program are two status bits: limit interrupt and lost count.

The enable clock and limit interrupt functions are selected by performing a write to the real-time clock (W = 0, E = 1, and S = 7) and setting the two least significant bits of the Q register equal to 1 ($Q = 00F3_{16}$). The enable clock and limit interrupt functions are disabled in the same manner with the two least significant bits of the Q register equal to 0 ($Q = 00F0_{16}$). Either case clears an existing limit interrupt and clears the status of the real-time clock.

The real-time clock status is obtained by an input from the real-time clock (W = 0, E = 1, and S = 7). Status is returned in the A register with bit 15 (when true) indicating a lost count and bit 14 (when true) indicating a limit interrupt. The rest of the bits in the A register are undefined.

The limit interrupt that is received by a macro-level program is dependent on the appropriate M register bit (M08, 1700 convention) being set and the macro interrupt enabled, as with all other 1700 peripherals.

The emulator is capable of receiving a micro interrupt from the real-time clock every 3-1/3 milliseconds (based on a crystal oscillator). This interrupt is enabled anytime the DMI instruction has defined the micro interrupt (INT08) and the clock has been enabled as indicated above.

The value stored for the clock limit in the auto-data transfer for the clock determines when the emulator generates the macro-level interrupt. If the emulator becomes overloaded with higher priority micro interrupts and the micro interrupt for the clock has not been cleared before another 3-1/3 millisecond count occurs (and the limit interrupt has been selected), then the lost count status bit is set. This causes a limit interrupt to occur with the lost count status bit set.

The real-time clock is always ready, and reads or writes are never rejected.

A FIELD – In a micro instruction, the A field specifies the operand source to be sent to the ALU from selector 1.

A REGISTER – General-purpose register

AB – Address buffer register; main memory address register

ALU – Arithmetic/logical unit; performs arithmetic and logical operations on two operands received from the two selectors.

AUTOLOAD – Process whereby main memory is loaded from an external input device via the memory DMA port

B FIELD – In a micro instruction, the B field specifies the operand source to be sent to the ALU from selector 2.

BG – Bit generator; allows a word containing all 0s except one bit at any position; used for masking or arithmetic operations.

BOUNDS REGISTERS – Two registers in main memory containing the upper and lower addresses forming the boundaries of the unprotected portion of memory.

C FIELD – Constant field micro-instruction field; may contain constants, micro-memory addresses, or other codes, depending on format of micro instruction

CHECK BIT – On a main memory with error checking and correction, one of five bits stored with each word that is decoded when read to locate single bit errors.

CPU – Central processing unit; consists of micro memory, control section, arithmetic section, and identification

D REGISTER – Data register on input/output card

D FIELD – Destination field/micro-instruction field; specifies the destination for results of the operation performed by ALU

DEADSTART – Optional logic that allows read/write micro memory to be loaded from the external input device

ECC – Error checking and correction; five check bits are stored with each word that are decoded to locate and correct single bit errors. Also, the instruction code for read error checking and correction status.

EMULATION – Process combining hardware and firmware design in which one processor (emulator) executes programs designed for a different processor, even though one-to-one hardware correspondence does not exist

1700 ENHANCED PROCESSOR – A 16-bit processing element operating as an enhanced CDC 1700 computer

F FIELD – Function field micro-instruction field; specifies the operation to be performed by ALU, shift, or scale of A or A/Q registers

F REGISTER – General purpose register

FILE 1 – Optional register file addressed by the contents of the K register

FILE 2 – Register file typically addressed by the contents of N register

FIRMWARE – General term for combination of micro instructions used in the micro program to perform a certain operation

I REGISTER – Storage location 00FF used for 1700 instruction indexing; also a general-purpose register used in 1700 simulation

IXT – I register external on the transform

I/O – Input/output

K REGISTER – Eight-bit counter that can be cleared, incremented, or decremented under micro-instruction control; also used to address file 1

M FIELD – Mode field micro-instruction field; specifies the addressing mode to be used to obtain the next micro-instruction pair from micro memory

MA REGISTER – Micro-memory address register; holds the micro-memory address of the current micro-instruction pair

MA TRANSFORM – Micro-memory address transform

MAC – Memory address counter; holds the address of the next sequential micro-instruction pair

MAIN MEMORY – Core memory used by the processor for storage of operands, etc.

MASK REGISTER – Used to control internal and external interrupt processing

MEMORY PAGE FILE – The page mode 0 and page mode 1 register files in main memory

MICRO INSTRUCTION – A 32-bit micro-memory instruction that controls all operations throughout the system

MICRO MEMORY – High-speed semiconductor memory that contains micro programs

MICRO PROGRAM – A set of micro instructions stored in micro memory

MIR – The micro-instruction register; holds the micro instruction being executed

MM – Micro memory

MOS – Metal oxide silicon; the process used to fabricate the semiconductor memory circuits

MP – Micro processor; the basic micro-programmable processor that can be configured in many forms/applications

N REGISTER – An eight-bit counter that can be cleared. incremented, or decremented under micro-instruction control; also used to address file 2

PAGE – In main memory, a section consisting of 2K words accessed through the memory page file

PAGE MODE – A method of indirect addressing with a 5-bit page address and 11-bit word address.

PAGE REGISTER – One of 64 registers in the memory page file containing a page address

P REGISTER – General-purpose register used to hold the main memory address of software instruction being executed if the processor is configured as emulator

PROGRAM PROTECT – Optional logic that, when enabled, prevents unprotected programs and I/O users from changing contents of protected areas of main memory

Q REGISTER – General-purpose register used in mulitplication and division operations

RTJ REGISTER – Return jumper register; holds the micro-memory address to which control returns at completion of a subroutine

SEC STATUS – Single error correction status; available to the processor on an ECC instruction

S FIELD – A special field in the micro-instruction field; specifies the operation to be performed in parallel with the ALU operation

S1, S2, ETC. – Selector 1, selector 2, etc.

SELECTOR – A multiplexer that allows one of several sources of data to be selected for transfer from one locaiton in the processor organization to another under control of the micro instruction

SM – Status/mode register; contains flag bits and status/mode bits. Flag bits are set under micro instruction control to enable certain internal processor operations. Status/mode bits indicate internal or external conditions (for example, memory parity error).

SMI CARD – Status mode interrupt module; contains the status mode registers, mask registers, and interrupt registers for the micro processor

SYNDROME BITS – A group of five bits derived from the ECC bits that identify a bit error

T FIELD – Test field in micro-instruction field; specifies if the upper or lower micro instruction of next micro-instruction pair is to be executed

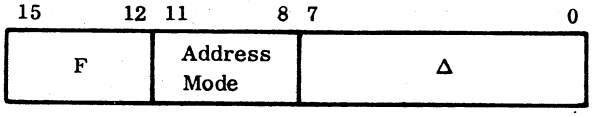
TRANSFORM MATRIX – Selects bits from various sources in the processor organization and translates them into micro-memory address in the MA register or transfers them to the K or N register

X REGISTER – Genreal-purpose processor register

Y REGISTER – Address register on the processor (1700) identification card

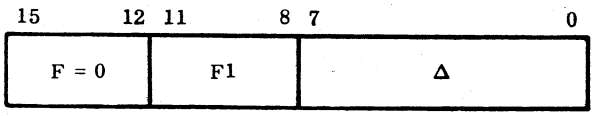
BASIC INSTRUCTIONS

STORAGE REFERENCE



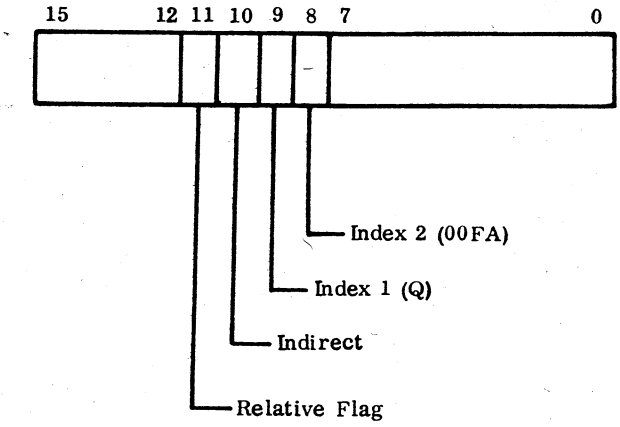
F = 1 JMP
F = 2 MUI
F = 3 DVI
F = 4 STQ
F = 5 RTJ
F = 6 STA
F = 7 SPA
F = 8 ADD
F = 9 SUB
F = A AND
F = B EOR
F = C LDA
F = D RAO
F = E LDQ
F = F ADQ

REGISTER REFERENCE



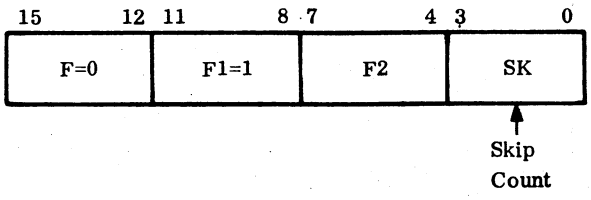
F1 = 0 SLS (Δ=0)
F1 = 1 SKIP
F1 = 2 INP
F1 = 3 OUT
F1 = 4 EIN (Δ=0)
F1 = 5 IIN (Δ=0)
F1 = 6 SPB (Δ=0)
F1 = 7 CPB (Δ=0)
F1 = 8 Inter-register
F1 = 9 INA
F1 = A ENA
F1 = B NOP (Δ=0)
F1 = C ENQ
F1 = D INQ
F1 = E EXI
F1 = F SHIFT

ADDRESS MODE



8-bit absolute:	0 to 3, Δ=0
8-bit absolute indirect:	4 to 7, Δ=0
8-bit relative:	8 to 11, Δ=0
8-bit relative indirect:	12 to 15, Δ=0
Absolute constant:	0 to 3, Δ=0
16-bit storage:	4 to 7, Δ=0
16-bit relative:	8 to 11, Δ=0
16-bit relative indirect:	12 to 15 Δ=0

SKIP FORMAT



F2 = 0 SAZ

F2 = 1 SAN

F2 = 2 SAP

F2 = 3 SAM

F2 = 4 SQZ

F2 = 5 SQN

F2 = 6 SQP

F2 = 7 SQM

F2 = 8 SWS

F2 = 9 SWN

F2 = A SOV

F2 = B SNO

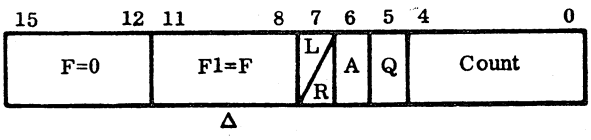
F2 = C SPE

F2 = D SNP

F2 = E SPF

F2 = F SNF

SHIFT FORMAT



010xxxxx ARS

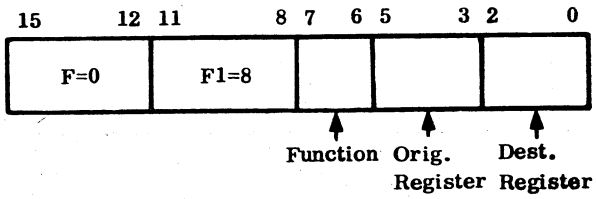
001xxxxx QRS

011xxxxx LRS

110xxxxx ALS

111xxxxx LLS

INTER-REGISTER FORMAT



76543

10000 SET

01000 CLP

10100 TRA

10010 TRQ

10011 TRB

01100 TCA

01001 TCM

01010 TCQ

01011 TCB

00101 AAM

00111 AAB

00110 AAQ

01101 EAM

01110 EAQ

01111 EAB

10101 LAM

10110 LAQ

10111 LAB

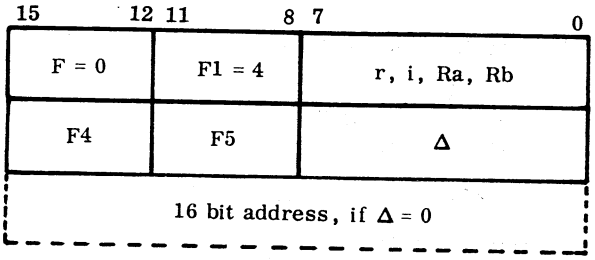
11101 CAM

11110 CAQ

11111 CAB

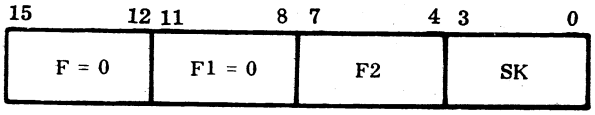
ENHANCED INSTRUCTIONS

ENHANCED STORAGE REFERENCE (r,i, Ra, Rb=0)



F4 = 5, F5 = 0, Rb = 0	SJE
F4 = 5, F5 = 0, Rb = 0	SJr
F4 = 8, F5 = 0, Rb = 0	ARr
F4 = 9, F5 = 0, Rb = 0	SBr
F4 = A, F5 = 0, Rb = 0	ANr
F4 = A, F5 = 1, Rb = 0	AMr
F4 = C, F5 = 0, Rb = 0	LRr
F4 = C, F5 = 1, Rb = 0	SRr
F4 = C, F5 = 2	LCA
F4 = C, F5 = 3	SCA
F4 = D, F5 = 0, Rb = 0	ORr
F4 = D, F5 = 1, Rb = 0	OMr
F4 = E, F5 = 0, Rb = 0	CrE
F4 = E, F5 = 2	CCE

ENHANCED SKIP INSTRUCTIONS



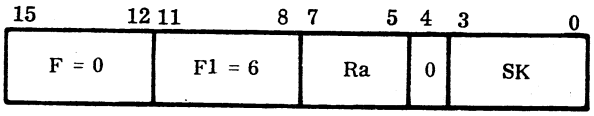
F2 = 0, 4, 8, or C SrZ SK
r = 4, 1, 2, or 3

F2 = 1, 5, 9, or D SrN SK
r = 4, 1, 2, or 3

F2 = 2, 6, A, or E SrP SK
r = 4, 1, 2, or 3

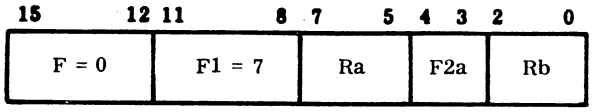
F2 = 3, 7, B or F SrM SK
r = 4, 1, 2, or 3

DECREMENT AND REPEAT



Ra = 1 to 7 DrP SK

ENHANCED INTER-REGISTER

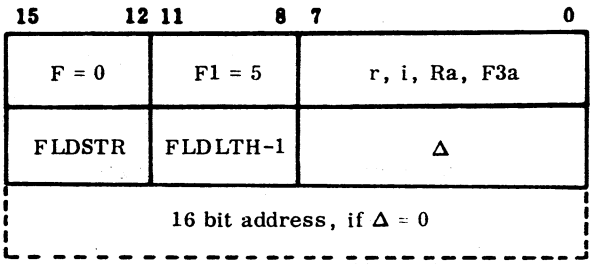


F2a = 0, Ra = 1-7 XFr R
Rb = 1-4, Q, A, I

NOTE

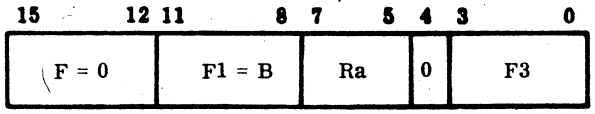
Ra, Rb (0 to 7) = 0, 1, 2, 3, 4, Q, A, I

FIELD REFERENCE



F3a = 2	SFZ
F3a = 3	SFN
F3a = 4	LFA
F3a = 5	SFA
F3a = 6	CLF
F3a = 7	SEF

MISCELLANEOUS



F3 = 1, Ra = 0 LMM

F3 = 2, Ra = 0 LRG

F3 = 3, Ra = 0 SRG

F3 = 4, Ra = 0 SIO

F3 = 5, Ra = 0 SPS

F3 = 6, Ra = 0 DMI

F3 = 7, Ra = 0 CBP

F3 = 8, Ra = 0 GPE

F3 = 9, Ra = 0 GPO

F3 = A, Ra = 0 ASC

F3 = B, Ra = 0 APM

F3 = C, Ra = 0 PM0

F3 = D, Ra = 0 PM1

F3 = 0, Ra = r LUB

F3 = 1, Ra = 4 LLB

F3 = 2, Ra = 4 EMS

F3 = 3, Ra = r WPR R

F3 = 4, Ra = 4 RPR R

F3 = 5, Ra = r ECC R

When calculating the instruction execution times listed on the following pages, the user must consider the following parameters:

1. For basic storage reference instructions, add the following addressing mode time to the execution time given in this appendix.

F1	Delta	Additional Execution Time	F1	Delta	Additional Execution Time
0	≠0	0.00	0	= 0	0.29
1		0.00	1		0.51
2		0.00	2		0.51
3		0.29	3		0.51
4		0.80	4		0.80
5		0.80	5		0.80
6		0.80	6		0.80
7		0.80	7		0.80
8		0.00	8		0.80
9		0.29	9		0.80
10		0.29	10		0.80
11		0.57	11		1.07
12		0.80	12		1.57
13		0.80	13		1.57
14		0.80	14		1.57
15		0.80	15		1.57

2. For an enhanced storage reference field instruction, add the following address mode time to the execution time given in this appendix.

Addressing Mode	Delta	Additional Execution Time
0	≠0	0.00
1		0.67
2		0.28
3		0.78

Addressing Mode	Delta	Additional Execution Time
0	=0	0.22
1		0.72
2		0.72
3		1.50

3. Add 0.72 microseconds for the following instructions:

SJI

ARJ

SBI

ANI

LRI

ORI

Mnemonic	Definition	Execution Times (μsec)	OP Code			
AAB	Transfer Arithmetic Sum A, Q+M	1.74, 1.91, 2.08, 2.25	0	8	3	8—F
AAM	Transfer Arithmetic Sum A, M	1.74, 1.91, 2.08, 2.25	0	8	2	8—F
AAQ	Transfer Arithmetic Sum A, Q	1.10, 1.34, 1.51, 1.54†	0	8	3	0—7
ADD	ADD A	1.76	8	0 to F	Δ	
ADQ	ADD Q	1.76	F	0 to F	Δ	
ALS	A Left Shift	1.62 + .056 * N	0	F	C/D	0—F
AMr	AND Memory	5.68	0	4	0 to F	0 to F
			A	1	Δ	
AND	AND with A	1.62	A	0 to F	Δ	
ANr	AND Register	5.40	0	4	0 to F	0 to F
			A	0	Δ	
ARr	Add Register	5.40	0	4	0 to F	0 to F
			8	0	Δ	
ARS	A Right Shift	1.62 + .056 * N	0	F	4/5	0—F
ASC	Accumulator Scale	2.88 + .056 * N	0	B	0	A
CAB	Transfer Complement Logical Product A, Q+M	1.63, 1.80, 1.96, 2.13†	0	8	F	8—F
CAM	Transfer Complement Logical Product A, M	1.63, 1.80, 1.96, 2.13†	0	8	E	8—F
CAQ	Transfer Complement Logical Product A, Q	1.18, 1.34, 1.34, 1.51†	0	8	F	0—7
CBP	Clear Breakpoint Interrupt	2.19	0	B	0	7
CCE	Compare Character Equal	6.14	0	4	0—F	0—F
			E	2	Δ	

†For inter-register instructions, the first execution time is for A or Q register destinations, the second time is for M, A and M, or Q and M registers, the third time is for A and Q, and the fourth time is for A and Q and M.

Mnemonic	Definition	Execution Times (μsec)	OP Code			
CLF	Clear Field	6.64	0 0 to F	5 0 to F	+ Δ	6
CLR	Clear to Zero	1.18, 1,34, 1.34, 1.51†	0	8	4	0 to 7
CPB	Clear Program Protect	1.72	0	7	0	0
CrE	Compare Register Equal	5.23, 5.46††	0 E	4 0	0 to F Δ	0 to F
DMI	Define Micro Interrupt	3.43	0	B	0	6
DrP	Decrement and Repeat	2.22†††	0	6	††††	0 to F
DVI	Divide Integer	10.48	3	0 to F	Δ	
EAB	Transfer Exclusive OR A, Q, M	1.63, 1.80, 1.96, 2.13†	0	8	7	8 to F
EAM	Transfer Exclusive OR A, M	1.63, 1.80, 1.96, 2.13†	0	8	6	8 to F
EAQ	Transfer Exclusive OR A, Q	1.18, 1.34, 1.34, 1.51†	0	8	7	0 to 7
EIN	Enable Interrupt	1.40	0	4	0	0
EMS	Execute Micro Sequence	6.20†††††	0	B	r, o	2
ENA	Enter A	.95	0	A	Δ	
ENQ	Enter Q	.95	0	C	Δ	
EOR	Exclusive OR with A	1.62	B	0 to F	Δ	
EXI	Exit Interrupt State	1.85	0	E	Δ	

†For inter-register instructions, the first execution time is for A or Q register destinations, the second time is for M, A and M, or Q and M registers, the third time is for A and Q, and the fourth time is for A and Q and M.

††For compare instructions, the first execution time listed is for unequal conditions, and the second time is for equal conditions.

†††Add .62 microseconds for the DIP instruction.

††††2, 4, 6, 8, A, C, E

†††††Plus micro-sequence time

Mnemonic	Definition	Execution Times (μsec)	OP Code			
GPE	Generate Character Parity Even	3.92	0	B	0	8
GPO	Generate Character Parity Odd	3.92	0	B	0	9
IIN	Inhibit Interrupt	1.40	0	5	0	0
INA	Increase A	.95	0	9		Δ
INP	Input to A	3.77 min. 15.63 max†	0	2		Δ
INQ	Increase Q	.95	0	D		Δ
JMP	Jump	1.17	1	0 to F		Δ
LAB	Transfer Logical Product A, Q+M	1.63, 1.80, 1.96, 2.13††	0	8	B	8 to F
LAM	Transfer Logical Product A, M	1.63, 1.80, 1.96, 2.13††	0	8	A	8 to F
LAQ	Transfer Logical Product A, Q	1.10, 1.34, 1.34, 1.51††	0	8	B	0 to 7
LCA	Load Character to A	5.80	0 C	4 2	0 to F	0 to F Δ
LDA	Load A	1.62	C	0 to F		Δ
LDQ	Load Q	1.62	E	0 to F		Δ
LFA	Load Field	6.19 + .056 * N	0 0 to F	5 0 to F	0 to F	4 or C Δ
LLB	Load Lower Unprotected Bounds	2.14	0	B	r, o	1
LLS	Long Left Shift	2.30 + .056 * N	0	F	E/F	0 to F
LMM	Load Micro Memory	2.42 + 3.5 * N	0	B	0	1
LRG	Load Registers	13.80	0	B	0	2

†Maximum time is for internal reject

††For inter-register instructions, the first execution time is for A or Q register destinations, the second time is for M, A and M, or Q and M registers, the third time is for A and Q, and the fourth time is for A and Q and M.

Mnemonic	Definition	Execution Times (μsec)	OP Code			
LRr	Load Register	5.40	0 C	4 0	0 to F Δ	0 to F
LRS	Load Right Shift	2.30 + .056 * N	0	F	6/7	0 to F
LUB	Load Upper Unprotected Bounds	2.14	0	B	r, o	0
MUI	Multiply Integer	5.62 min. 7.49 max.	2	0 to F	Δ	
NOP	No Operation	1.17	0	F	0 to 1	0 to F
OMr	OR Memory	5.68	0 D	4 1	0 to F Δ	0 to F
ORr	OR Register	5.40	0 D	4 0	0 to F Δ	0 to F
OUT	Output from A	3.49 min. 15.63 max. †	0	3	Δ	
QLS	Q Left Shift	1.96 + .056 * N	0	F	A or B	0 to F
QRS	Q Right Shift	1.96 + .056 * N	0	F	2 or 3	0 to F
PMO	Page Mode O	xx	0	B	0	C
PMI	Page Mode 1	xx	0	B	0	C
RAO	Replace Add 1 in Storage	2.22	D	0 to F		
RPR R	Read Page Register	xx	0	B	r, 0	4
RTJ	Return Jump	1.69	5	0 to F	Δ	
SAM	Skip if A = -	1.23, 1.52††	0	1	3	0 to F
SAN	Skip if A ≠ +0	1.23, 1.52††	0	1	1	0 to F
SAP	Skip if A = +	1.23, 1.52††	0	1	2	0 to F
SAZ	Skip if A = +0	1.23, 1.52††	0	1	0	0 to F
SBr	Subtract Register	5.47	0 9	4 0	0 to F Δ	0 to F
SCA	Store Character from A	6.53	0 C	4 3	0 to F Δ	0 to F

†Maximum time is for internal reject

††For skip instructions, the first execution time is for no skip, and the second is for skip.

Mnemonic	Definition	Execution Times (μsec)	OP Code			
SEF	Set Field	6.64	0 0 to F	5 0 to F	0 to F Δ	7 or F
SET	Set to 1s	1.18, 1.34, 1.34, 1.51†	0	8	8	0 to 7
SFA	Store Field	7.15 * .056N	0 0 to F	5 0 to F	0 to F Δ	5 or D
SFN	Skip if Field Nonzero	5.85, 6.08††	0 0 to F	5 0 to F	0 to F Δ	3 or B
SFZ	Skip if Field Zero	5.85, 6.08††	0 0 to F	5 0 to F	0 to F Δ	2 or A
SIO	Set/Sample Output or Input	3.88	0	B	0	4
SJE	Subroutine Jump Exit	4.50	0 5	4 0	0 to F Δ	0 to F
SJr	Subroutine Jump	4.67	0 5	4 0	0 to F Δ	0 to F
SLS	Select Stop	1.35	0	0	0	0
SNF	Skip on No Program Protect Fault	1.17, 1.46††	0	1	B	0 to F
SNO	Skip on No Overflow	1.17, 1.46††	0	1	F	0 to F
SNP	Skip on No Storage Parity Error	1.35, 1.46††	0	1	D	0 to F
SOV	Skip on Overflow	1.17, 1.46††	0	1	A	0 to F
SPA	Store A, Parity to A	2.18	7	0 to F	Δ	
SPB	Set Program Protect	1.72	0	6	0	0
SPE	Skip on Storage Parity Error	1.35, 1.46††	0	1	C	0 to F
SPF	Skip on Program Protect Fault	1.17, 1.46††	0	1	E	0 to F

†For inter-register instructions, the first execution time is for A or Q register destinations, the second time is for M, A and M, or Q and M registers, the third time is for A and Q, and the fourth time is for A and Q and M.

††For skip instructions, the first execution time is for no skip, and the second is for skip.

Mnemonic	Definition	Execution Times (μsec)	OP Code			
SPS	Sample Position Status	3.94	0	B	0	5
SQM	Skip if Q = -	1.23, 1.52†	0	1	7	0 to F
SQN	Skip if Q ≠ +0	1.23, 1.52†	0	1	5	0 to F
SQP	Skip if Q = +	1.23, 1.52†	0	1	6	0 to F
SQZ	Skip if Q = +0	1.23, 1.52†	0	1	4	0 to F
SRG	Store Registers	12.59	0	B	0	3
SrM	Skip if Register Negative	1.91, 2.02†	0	0	3, 7 B, F	0 to F
SrN	Skip if Register Nonzero	1.91, 2.02†	0	0	1, 5 9, D	0 to F
SrP	Skip if Register Positive	1.91, 2.02†	0	0	2, 6 A, E	0 to F
SRr	Store Register	5.51	0 C	4 1	0 to F	0 to F Δ
SrZ	Skip if Register Zero	1.91, 2.02†	0	0	0, 4 8 C	0 to F
STA	Store A	1.69	6	0 to F	Δ	
STQ	Store Q	1.69	4	0 to F	Δ	
SUB	Subtract	1.76	9	0 to F	Δ	
SWN	Skip if Switch not Set	1.12, 1.40†	0	1	9	0 to F
SWS	Skip if Switch Set	1.12, 1.40†	0	1	8	0 to F
TCA	Transfer Complement A	1.18, 1.34, 1.34, 1.51††	0	8	6	0 to 7
TCB	Transfer Complement Q+M	1.46, 1.62, 1.79, 1.96††	0	8	5	8 to F

† For skip instructions, the first execution time is for no skip, and the second is for skip.

†† For inter-register instructions, the first execution time is for A or Q register destinations, the second time is for M, A and M, or Q and M registers, the third time is for A and Q, and the fourth time is for A and Q and M.

Mnemonic	Definition	Execution Times (μsec)	OP Code			
TCM	Transfer Complement M	1.46, 1.62, 1.79, 1.96†	0	8	4	8 to F
TCQ	Transfer Complement Q	1.18, 1.34, 1.34, 1.51†	0	8	5	0 to 7
TRA	Transfer A	1.18, 1.34, 1.34, 1.51†	0	8	A	0 to 7
TRB	Transfer Q+M	1.46, 1.62, 1.79, 1.96†	0	8	9	8 to F
TRM	Transfer M	1.46, 1.62, 1.79, 1.96†	0	8	8	8 to F
TRQ	Transfer Q	1.18, 1.34, 1.34, 1.51†	0	8	9	0 to 7
XFr	Transfer Register	2.47††	0	7	0, 1 to 7	1 to 7

†For inter-register instructions, the first execution time is for A or Q register destinations, the second time is for M, A and M, or Q and M registers, the third time is for A and Q, and the fourth time is for A and Q and M.

††Add .67 microseconds for XFI instruction.

COMMENT SHEET

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(Macro Level) Reference Manual

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